SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY

Department of Electrical and Electronics Engineering	LP: EE22308
B.E/~~B.Tech/M.E/M.Tech~~ : EEE Regulation: R2022	Rev. No: 00
PG Specialisation :NA	Date: 31.07.2023
Sub. Code / Sub. Name : **EE22308 - DIGITAL LOGIC CIRCUITS: THEORY AND PRACTICES**	
Unit : 1	

UNIT I NUMBER SYSTEMS, CODES AND BOOLEAN REDUCTION

Review of number systems, Signed binary numbers – Binary Arithmetic – Fixed and floating pointer presentation – Boolean Algebra - laws and theorems – Simplification of Boolean expressions–Sum of Products (SOP) and Product of Sums (POS) forms – Logic Minimization using K-map – Binary codes–BCD code, Gray code, Error detection and Error correction codes.

Experiments:

1. Reduction and Implementation of Boolean Expression using logic gates (K-map).
2. Implementation of Code Converters (Binary to Gray, and Gray to Binary) using logic gates

Objective:

To impart knowledge on concepts of binary representation, logic gates, and Boolean algebra..

Session No *	Topics to be covered	Ref	Teaching Aids
1	Review of number systems	1,2,3	PPT, BB
2	Signed binary numbers – Binary Arithmetic	1,2,3	PPT, BB
3	Fixed and floating pointer presentation -Boolean Algebra - laws and theorems	1,2,3	PPT, BB
4	Simplification of Boolean expressions–Sum of Products (SOP)	1,2,3	PPT, BB
5	Simplification of Boolean expressions -Product of Sums (POS) forms	1,2,3	PPT,BB
6	Logic Minimization using K-map	1,2,3	PPT, BB
7, 8, 9	Practice session on Reduction and Implementation of Boolean Expression using logic gates (K-map).	1,2,3	BB / Hands on
10	Simplification of Boolean expressions -Product of Sums (POS) forms	1,2,3	PPT, BB
11	Binary codes–BCD code, Gray code	1,2,3	PPT, BB
12	Error detection and Error correction codes.	1,2,3	PPT, BB
13,14, 15	Practice session on Implementation of Code Converters (Binary to Gray, and Gray to Binary) using logic gates	1,2,3	BB / Hands on
Content beyond syllabus covered (if any):			

* Session duration: 50 minutes

SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY

Sub. Code / Sub. Name: **EE22308 DIGITAL LOGIC CIRCUITS: THEORY AND PRACTICES**

Unit : II

UNIT II COMBINATIONAL CIRCUITS

Combinational logic – Adders, Ripple carry adder, Carry lookahead adder, Subtractor, Multiplexer, Demultiplexer, Encoder, Decoder, Parity generator and checker – Introduction to VHDL coding. Experiments:

1. Implementation of Adder and Multiplexer.
2. Design and simulation of Adder/ Subtractor circuits.
3. Design and simulation of Multiplexer and Demultiplexer.

Objective:

To design and analyze digital circuits using combinational and sequential logic
To develop skills in HDL coding and simulate digital circuits.

Session No *	Topics to be covered	Ref	Teaching Aids
16	Combinational logic circuit introduction	1,2,3	PPT, BB
17	Adders, Ripple carry adder	1,2,3	PPT, BB
18	Carry lookahead adder	1,2,3	PPT, BB
19	Full Adder and Full Subtractor	1,2,3	PPT, BB
20, 21, 22	Implementation of Adder and Multiplexer	1,2,3	BB / Hands on
23	Multiplexer, Demultiplexer	1,2,3	PPT, BB
24	Encoder, Decoder, Parity generator and checker	1,2,3	PPT, BB
25, 26, 27	Design and simulation of Adder/ Subtractor circuits	1,4,7	BB / Hands on
28	Introduction to VHDL coding	1,4,7	PPT, BB
28,29,30	Design and simulation of Multiplexer and Demultiplexer	1,4,7	BB / Hands on
Content beyond syllabus covered (if any): **Booth Multiplier**			

* Session duration: 50 mins

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Unit : III

UNIT-III SEQUENTIAL CIRCUITS

Sequential logic – SR, JK, D and T flip flops –Synchronous counter – Ripple Counter – Modulo-n counter–Sequence generator – Design of synchronous sequential circuits – Moore and Mealy models–state diagram, state reduction, state assignment.
Experiments:
1. Implementation and simulation of Shift registers.
2. Design, implementation and simulation of Synchronous counter.

Objective:
To design and analyze digital circuits using sequential logic.

Session No *	Topics to be covered	Ref	Teaching Aids
31	Introduction to Sequential circuits	1,2,3	PPT,BB
32	SR and D flip flops	1,2,3	PPT,BB
33	JK and T flip flops	1,2,3	PPT,BB
34,35, 36	Implementation and simulation of Shift registers.	1,2,3	BB / Hands on
37	Synchronous counter	1,2,3	PPT/Hands on training
38	Ripple Counter	1,2,3	PPT,BB
39	Modulo-n counter	1,2,3	PPT,BB
40	Sequence generator, Design of synchronous sequential circuits	1,2,3	PPT,BB
41	Moore and Mealy models–state diagram	1,2,3	PPT,BB
42	State diagram, state reduction, state assignment	1,2,3	PPT,BB
43,44, 45	Design, implementation and simulation of Synchronous counter	1,2,3	BB / Hands on

Content beyond syllabus covered (if any):

Realization of One Flip-Flop using Other Flip-Flops

SR Flip-Flop to D Flip-Flop , SR Flip-Flop to JK Flip-Flop, JK Flip-Flop to T Flip-Flop

JK Flip-Flop to D Flip-Flop , D Flip-Flop to T Flip-Flop , T Flip-Flop to D Flip-Flop

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Unit : IV

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

Design of Asynchronous sequential circuits – Transition table, flow table – race conditions, hazards and errors in digital circuits; Analysis of asynchronous sequential logic circuits – Design of asynchronous controller for vending machine.

Experiments: 1. Design, implementation and simulation of Asynchronous counter.

Objective:

To design and analyze digital circuits using sequential logic

Session No *	Topics to be covered	Ref	Teaching Aids
46	Design of Asynchronous sequential circuits	1,2,3	PPT,BB
47	Design of Asynchronous sequential circuits	1,2,3	PPT,BB
48	Transition table, flow table	1,2,3	PPT,BB
49	Transition table, flow table	1,2,3	PPT,BB
51	Race conditions, hazards and errors in digital circuits	1,2,3	PPT,BB
52	Race conditions, hazards and errors in digital circuits	1,2,3	PPT,BB
53	Analysis of asynchronous sequential logic circuits	1,2,3	PPT,BB
54	Analysis of asynchronous sequential logic circuits	1,2,3	PPT,BB
55, 56 , 57	Design, implementation and simulation of Asynchronous counter	1,2,3	BB / Hands on
58	Design of asynchronous controller for vending machine	1,2,3	PPT,BB
59	Design of asynchronous controller for vending machine	1,2,3	PPT,BB
60	Discussion of Asynchronous sequential circuits	1,2,3	PPT,BB
Content beyond syllabus covered (if any):			

SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY

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Unit : V

UNIT V MEMORY DEVICES AND DIGITAL LOGICAL FAMILIES

Implementation of combinational logic circuits using PROM, PLA, PAL – Introduction to FPGA– Digital Logic Families: Logic gates using TTL, ECL and MOS families – operation and characteristics of digital logical family.

Experiments:

1. Implementation and verification of two input NOR and NAND gates using TTL / CMOS

Objective:

To design and analyze digital circuits using sequential logic.

Session No *	Topics to be covered	Ref	Teaching Aids
61, 62	Implementation of combinational logic circuits using PROM,	1,2,3	PPT, BB
63,64	Implementation of combinational logic circuits using PLA,	1,2,3	PPT, BB
65, 66	Implementation of combinational logic circuits using PAL	1,2,3	PPT, BB
67	Introduction to FPGA	1,2,3	PPT, BB
68	Digital Logic Families: Logic gates using TTL- operation and characteristics	1,2,3	PPT, BB
69	Digital Logic Families: Logic gates using ECL– operation and characteristics of digital logical family.	1,2,3	PPT, BB
70	Digital Logic Families: Logic gates using ECL– operation and characteristics of digital logical family.	1,2,3	PPT, BB
71, 72	Digital Logic Families: Logic gates using MOS families – operation and characteristics of digital logical family	1,2,3	PPT, BB
73,74, 75	Implementation and verification of two input NOR and NAND gates using TTL/CMOS	1,2,3	BB / Hands on

Content beyond syllabus covered (if any):

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REFERENCES:

1.M. Morris Mano, 'Digital Design with an introduction to the VHDL', PearsonEducation,2013.

2.John M.Yarbrough, 'Digital Logic, Application & Design', Thomson, 2012.

3. Salivahanan, Arivazhagan, 'Digital Circuits & Design', Vikas Publishing House, 2012.

4. William Kleitz, 'Digital Electronics-A Practical Approach with VHDL', Pearson, 2014.

5. Floyd and Jain, 'Digital Fundamentals', 8th edition, Pearson Education, 2013.

6. Anand Kumar, 'Fundamentals of Digital Circuits', PHI,2013.

7. Gaganpreet Kaur, 'VHDL Basics to Programming', Pearson, 2013. 6. Mandal, 'Digital Electronics Principles & Application', McGraw Hill Education, 2014

	Prepared by	Approved by
Signature	KR. Santha	KR. Santha
Name	Dr.KR.Santha Mr.D.S.Purushothaman	Dr.KR.Santha
Designation	Vice Principal, Professor & HoD /EEE AP/EEE	Vice Principal, Professor & HoD /EEE
Date	31.7.23	31.7.23
Remarks *:		
Remarks *:		

* If the same lesson plan is followed in the subsequent semester/year it should be mentioned and signed by the Faculty and the HOD