SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY

Department of Information Technology	LP: IT22201
~~B.E~~/B.Tech~~/M.E/M.Tech~~ : Information Technology Regulation: 2022	Rev. No: 01
PG Specialisation : NA	Date: 03-02-2025
Sub. Code / Sub. Name : IT22201 – Computer Organization and Architecture.	
Unit : I	

Unit Syllabus: BASIC COMPUTER ORGANIZATION AND DESIGN 9

Instruction codes, Computer registers, computer instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-output and interrupt, Complete computer description, Design of Basic computer, design of Accumulator Unit.

Objective:
To make students understand the basic structure and operation of digital computer. To understand the hardware-software interface.

Session No *	Topics to be covered	Ref	Teaching Aids
1	Instruction codes	T1, Ch.5 (Pg.no. 123-128)	BB/PPT
2	Computer registers	T1, Ch.5 (Pg.no. 129-132)	BB/PPT
3	Computer instructions	T1, Ch.5 (Pg.no. 132-135)	BB/PPT
4	Timing and Control	T1, Ch.5 (Pg.no. 135-139)	BB/PPT
5	Instruction cycle	T1, Ch.5 (Pg.no. 139-150)	Mind mapping (Active Learning)
6	Memory-Reference Instructions	T1, Ch.5 (Pg.no. 139-150)	BB/PPT
7	Input-output and interrupt	T1, Ch.5 (Pg.no. 150-157)	BB/PPT
8	Complete computer description, Design of basic computer	T1, Ch.5 (Pg.no. 150-157)	BB/PPT
9	Design of Accumulator Unit	T1, Ch.5 (Pg.no. 157-167)	BB/PPT
Content beyond syllabus covered (if any):			

* Session duration: 50 minutes

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Sub. Code / Sub. Name: IT22201 – Computer Organization and Architecture.

Unit : II

Unit Syllabus: ALU AND CU 9

ALU - Addition and subtraction – Multiplication – Division – Floating Point operations –Subword parallelism. CPU- General Register Organization, Stack Organization, Instruction format, Addressing Modes, data transfer and manipulation, Program Control, Reduced Instruction Set Computer (RISC).

Objective:

To familiarize the student with arithmetic and logic unit and implementation of fixed point and floating point arithmetic operations.

Session No *	Topics to be covered	Text	Teaching Aids
10	ALU - addition and subtraction	T1, Ch.3 (Pg.no. 176-183)	Vlab (Experiential Learning)
11	Multiplication – Division	T1, Ch.3 (Pg.no. 183-196)	BB/PPT
12	Floating Point operations – Subword parallelism	T1, Ch.3 (Pg.no. 196-224)	BB/PPT
13	General register organization	T1, Ch.3 (Pg.no. 243-249)	BB/PPT
14	Stack organization	T1, Ch.3 (Pg.no. 249-257)	BB/PPT
15	Instruction format	T1, Ch.3 (Pg.no. 257-268)	BB/PPT
16	Addressing modes	T1, Ch.3 (Pg.no. 257-268)	BB/PPT
17	Data transfer and manipulation, Program control	T1, Ch.3 (Pg.no. 268-284)	BB/PPT
18	Reduced Instruction Set Computer (RISC)	T1, Ch.3 (Pg.no. 284-293)	BB/PPT
Content beyond syllabus covered (if any):			

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Sub. Code / Sub. Name: IT22201 – Computer Organization and Architecture.

Unit : III

Unit Syllabus: PIPELINING AND HAZARDS 9

Basic MIPS implementation – Building datapath – Control Implementation scheme – Pipelining – Pipelined datapath and control – Handling Data hazards & Control hazards – Exceptions, The ARM Cortex-A8 and Intel Core i7 Pipelines.

Objective:

To expose the students to the concept of pipelining.

Session No *	Topics to be covered	Text	Teaching Aids
19	Basic MIPS implementation	T1, Ch.4 (Pg.no. 244-251)	BB/PPT
20	Building data path	T1, Ch.4 (Pg.no. 251-259)	BB/PPT
21	Control implementation scheme	T1, Ch.4 (Pg.no. 259-269)	BB/PPT
22	Pipelining	T1, Ch.4 (Pg.no. 272-286)	BB/PPT
23	Pipelined data path and control	T1, Ch.4 (Pg.no. 300-303)	BB/PPT
24	Handling Data hazards & Control hazards	T1, Ch.4 (Pg.no. 303-312)	BB/PPT
25	Exceptions	T1, Ch.4 (Pg.no. 303-312)	BB/PPT
26	The ARM Cortex	T1, Ch.4 (Pg.no. 313-320)	Vlab (Experiential Learning)
27	A8 and Intel Core i7 pipelines	T1, Ch.4 (Pg.no. 313-320)	BB/PPT
Content beyond syllabus covered (if any):			

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Sub. Code / Sub. Name: IT22201 – Computer Organization and Architecture.

Unit: IV

Unit Syllabus: MEMORY AND I/O SYSTEMS 9

Memory hierarchy - Memory technologies – Cache basics – Measuring and improving cache performance - Input/output system, programmed I/O, DMA and interrupts, I/O processors.

Objective:

To familiarize the students with hierarchical memory system including cache memory and virtual memory.

Session No *	Topics to be covered	Ref	Teaching Aids
28, 29	Memory hierarchy	T1, Ch.5 (Pg.no. 373-378)	BB/PPT
30	Memory technologies	T1, Ch.5 (Pg.no. 378-383)	BB/PPT
31	Cache basics	T1, Ch.5 (Pg.no. 383-398)	BB/PPT
32	Measuring and improving cache performance	T1, Ch.5 (Pg.no. 398-418)	Vlab (Experiential Learning)
33	Input/output system	T1, Ch.4 (Pg.no. 377-380)	BB/PPT
34	Programmed I/O	T1, Ch.4 (Pg.no. 224-398)	BB/PPT
35	DMA and interrupts	T1, Ch.4 (Pg.no. 228-242)	BB/PPT
36	I/O processors	T1, Ch.4 (Pg.no. 242-253)	BB/PPT
Content beyond syllabus covered (if any):			

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Sub. Code / Sub. Name: IT22201 – Computer Organization and Architecture.
Unit : V

Unit Syllabus: MULTICORES, MULTIPROCESSORS, AND CLUSTERS 9

Shared Memory Multiprocessors, Hardware Multithreading, SISD, MIMD, SIMD, SPMD, and Vector, Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers, and Other Message-Passing Multiprocessors.

Objective:

To expose the students with different ways of communicating with I/O devices and standard I/O interfaces.

Session No *	Topics to be covered	Ref	Teaching Aids
37	Shared memory multiprocessors	T1, Ch.6 (Pg.no. 519-524)	BB/PPT
38	Hardware multithreading	T1, Ch.6 (Pg.no. 519-524)	BB/PPT
39	SISD – MIMD	T1, Ch.6 (Pg.no. 509-515)	BB/PPT
40	SIMD – SPMD	T1, Ch.6 (Pg.no. 509-515)	BB/PPT
41	Vector	T1, Ch.6 (Pg.no. 509-515)	BB/PPT
42	Introduction to Graphics Processing Units	T1, Ch.6 (Pg.no. 524-530)	Fish Bowl Activity (Active Learning Methodology)
43	Clusters	T1, Ch.6 (Pg.no. 531-536)	BB/PPT
44	Warehouse scale computers	T1, Ch.6 (Pg.no. 531-536)	BB/PPT
45	Other message-passing multiprocessors	T1, Ch.6 (Pg.no. 531-536)	BB/PPT
Content beyond syllabus covered (if any):			

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TEXT BOOKS:

1 David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014.

REFERENCES:

1.V. Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, "Computer Organisation", VI edition, McGraw-Hill Inc, 2012.
2.William Stallings "Computer Organization and Architecture", Seventh Edition, Pearson Education, 2006.
3.Vincent P. Heuring, Harry F. Jordan, "Computer System Architecture", Second Edition, Pearson Education, 2005.
4.Govindarajalu, "Computer Architecture and Organization, Design Principles and Applications", first edition, Tata McGraw Hill, New Delhi, 2005.
5. John P. Hayes, "Computer Architecture and Organization", Third Edition, Tata McGraw Hill, 1998.
6. http://nptel.ac.in/.

	Prepared by	Approved by
Signature	N.S. V.	3/2/25
Name	Mr. N. Selvaganesh Mr.V.Praveenkumar	Dr.V.Vidhya
Designation	Assistant Professor Assistant Professor	Professor & Head
Date	03.02.2025	03.02.2025
Remarks *:	same lesson plan is followed as previous year(2023-24)	

* If the same lesson plan is followed in the subsequent semester/year it should be mentioned and signed by the Faculty and the HOD