JANUARY 2025 VOL.5 ISSUE 1

Sri Venkateswara College of Engineering

CIRCUIT TIMES

INSIGHTS

- Faculty Article
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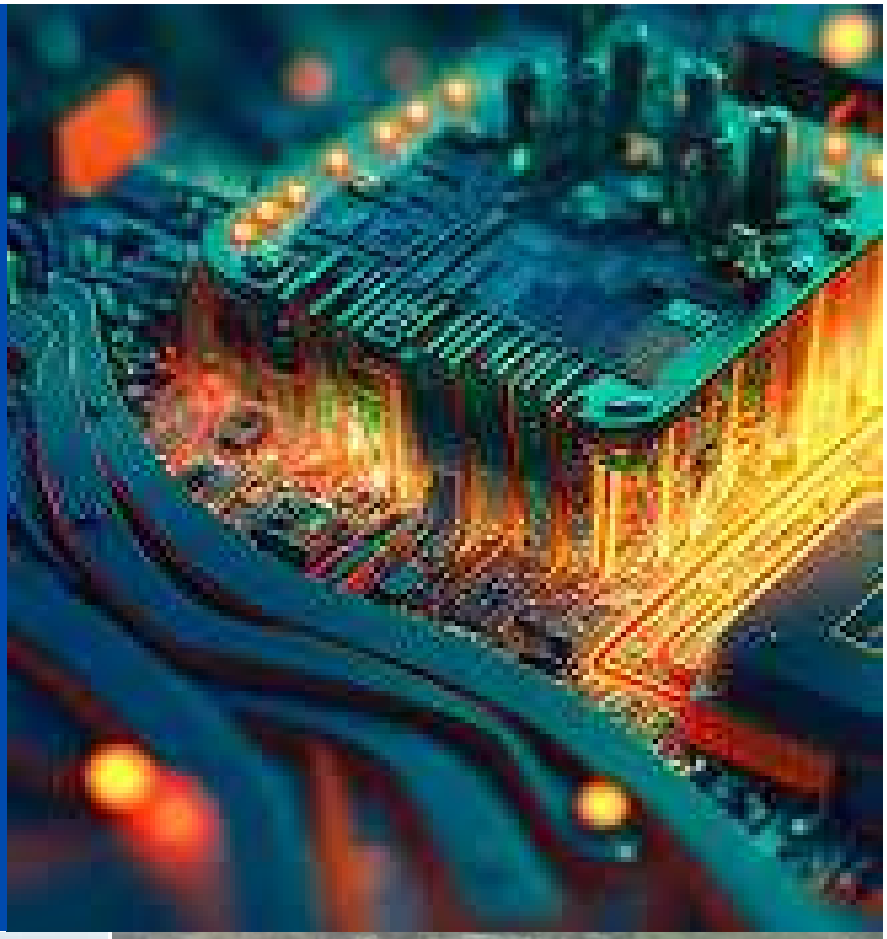
- Republic Day Celebration
- Student Participation
- Student Awards
- Internship Training
- Placement Activities
- BIS Activities
- Alumni Activities
- Alumni Achievements
- Alumni Testimonial



VISION OF DEPARTMENT

To lead the future of Electronics and Communication Engineering, through developing accomplished people, transformative research, distinguished academics, developing break-through innovations and sustainable solutions to serve society at the national and global level.

MISSION OF DEPARTMENT

By fostering a culture of continuous learning and knowledge acquisition in electronics and communication engineering through rigorous academic programs, research opportunities, industry collaborations, with provision of necessary resources and support.

By nurturing an environment that empowers learners to progress and reach their full potential, contributing to the advancement of Electronics and Communication Engineering and prosper in their careers.

By contributing to society through innovative and sustainable engineering solutions to tackle national and global issues, thereby enhancing the quality of lives and communities.

FACULTY ARTICLE

DIGITAL TRANSCEIVER USING H-TERNARY LINE CODING TECHNIQUE

Mr.A.Mahadevan,
Assistant Professor, Department of Electronics and Communication Engineering,
Sri Venkateswara College of Engineering (Autonomous), Sriperumbudur

1. INTRODUCTION

The digital transceiver using H-ternary line code is designed for base band transmission. The aim of this transceiver is sending and receiving the digital data between the computers in the wired and/or wireless networks like as LAN, WAN, MAN and ISDN etc. Every computer has a Network Interface Card (NIC) with unique address. The NIC card consists of a digital base band transceiver. The H-ternary line coding is able to work for this transceiver.

Ternary code

The line codes are classified into three different ways. The first approach is based on the number of levels in the coded output. They are named as binary, ternary and quaternary line codes. The binary line code has two output levels (+1 and 0), ternary line code has three output levels (+1, 0, -1) and the quaternary line code has four output levels.

2. PN SEQUENCE

The PN code sequence is a Pseudo-Noise or Pseudo-Random sequences of 1's and 0's, but not a real random sequence (because periodic). Random signals cannot be predicted. The PN sequence is obtained by using the D type flip flops. The length of the PN sequence is calculated from the formula, PNLength = 2(m) – 1. So, the length of the PN sequence will be 15. This PN sequence is considered as an input signal for the encoder.

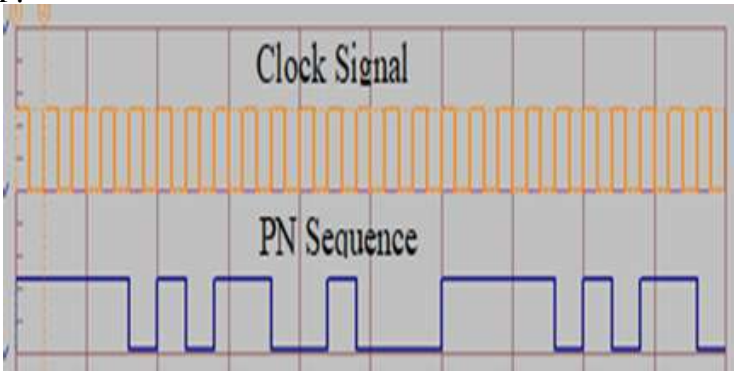


Fig.1. Generation of PN Sequence

2.1.Encoder

This code is working on the basis of hybrid principle that combines three binary codes. The polar NRZ (NRZ-L), dicode NRZ and Polar RZ codes are involved in the Hybrid Ternary line coding. Three levels are used to represent the H-Ternary output. These are positive (+), negative (-) and zero (0). The output state of the line code is in any one of the three levels. The state of the next level of the line code is depends on the input binary 1 or 0 and present state of the line code. There is no mathematical relation between this H-ternary line code and the basic three codes NRZ-L, dicode NRZ and polar RZ codes.

The function of the encoder is states as follows,

(i)The encoder produces + level when the input is a binary 1 whether the encoder output present state is at 0 or – level.

(ii)The encoder produces as – level when the input is a binary 0 whether the encoder output present state is at 0 or + level.

(iii)The encoder produces 0 level when the input is binary 1 and the encoder present state is + level or when the input is binary 0 and the encoder present state is – level.

(iv)Initially, the encoder output present state is assumed at 0 level when the first bit arrived at the encoder input.

In order to design the encoder these two variables are needed to written in Boolean expression. The Boolean expression of the next state Bn and Cn for a binary input A is calculated by using K-map. From the K-map the value of Bn and Cn obtained as Bn=AB'P and Cn=A'C'p. The Boolean expressions are implemented using the combinational logic circuits. A flip-flop is used for each as a feedback link between present and next binary states Bn and Cn. Then the final encoded output is obtained from subtracting Bp from Cp. This output will be the desired three levels signal H-ternary code. The circuit diagram of hybrid ternary line encoder is as shown in fig.2.

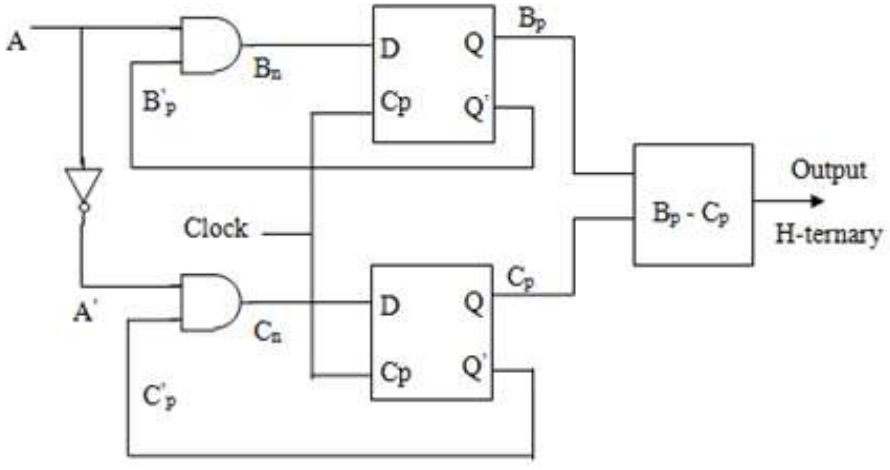


Fig.2. Hybrid Ternary Line Encoder

2.2.Decoder

The decoding is a reverse process of the encoding operation. The decoder input is in the form of three bit H-ternary code and its output is a two state binary signal. The function of the decoder is states as follows.

(i)The decoder produces an output binary 1 when the input ternary is at + level and whether the decoder output present state is a binary 1 or 0.

(ii)The decoder also produces an output binary 1 when the input ternary is at 0 level and the decoder output present state is at a binary 1.

(iii)The decoder produces an output binary 0 when the input ternary is at – level and whether the decoder output present state is a binary 0 or 1.

(iv)The decoder also produces an output binary 0 when the input ternary is at – level and the decoder present state is binary 0.

3. CLOCK RECOVERY CIRCUIT

The clock recovery circuit is very important to perform the proper decoding operation. The transmitter should be synchronies with the receiver to obtain the exact replica of the transmitted signal. In the decoder section, the clock signal to be generated accurately from the encoded signal. For this application, clock recovery circuit is employed. The clock recovery circuit is constructed by op-amp and timer ICs. The simulation results of clock recovery and received PN sequence signals are as shown in fig.3.

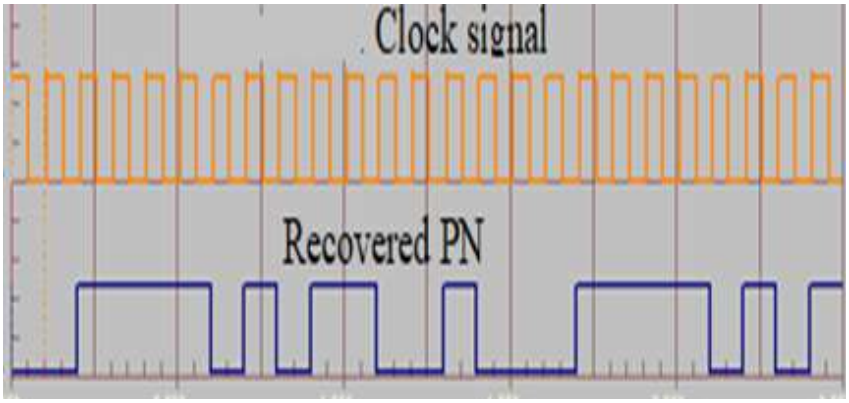


Fig.3.Received PN output

4. IMPLEMENTATION

The digital transceiver using hybrid ternary line coding system is designed and implemented in hardware using discrete components. And obtained the output signals and analyzed.

The PN signal and hybrid ternary encoder output signals are obtained in CRO as shown in fig. 4. and the recovered PN signal in the decoder is as shown in fig. 5.

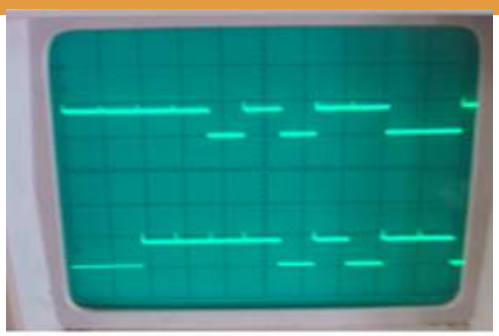


Fig.4.PN signal and Encoder output

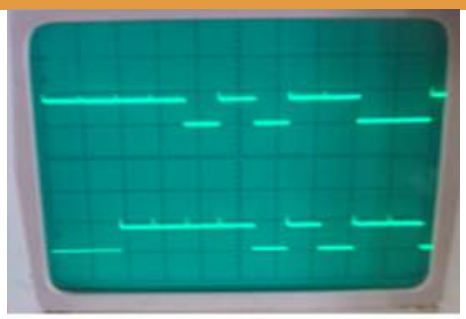


Fig.5.Recovered PN signal

5. CONCLUSION

Digital transceiver using H-ternary line coding is designed and implemented. Two set of encoder and decoder are assembled and data was communicated between the transceivers. The transceiver circuit was simulated as well as implemented by hardware. The results obtained in the simulation and hardware implementation are identical to each other. The decoded signal has two bit time delay with respect to the transmitted signal. This is because of using memory elements in the circuit. Encoder has one flip flop, so the one bit time delay will occur between encoded signal and input signal. The Power Spectral Density (PSD) is calculated using mathematical statistical for H-ternary line code and other codes like as polar NRZ, bipolar NRZ, Manchester NRZ, unipolar NRZ and bipolar RZ.

The PSD is analyzed by MATLAB programming. The PSD of the H-ternary line code over performs NRZ-L and lies between Bipolar RZ and Manchester line codes spectra. This H-ternary line codes is suitable for both pass band and base band data transmission. FSK modem is ican be used as a MODEM in computer networks.

REFERENCES

[1] Glass.A.Ali and Bastaki.E, “Design and modeling of H-Ternary line encoder for digital data transmission”, International Conference on Info-Tech & Info-Net, Beijing, China, 2001, pp 503-507.

[2] Glass.A.Ali and Abdulaziz,N, “H-Ternary line decoder for digital data transmission: circuit design and modeling”, 6th International Symposium on Digital Signal Processing for Communication Systems, Sydney, Australia, 2002, pp. 149-153.

[3] Takasaki.Y, “Digital Transmission Design and Jitter Analysis”, Artech House, 1991, pp.35-60.

[4] Couch.L.W, “Digital and Analog Communication Systems”, Prentice Hall, 1997, pp.127-225, 295-354.

FACULTY PARTICIPATION

(SEMINAR/FDP/STTP/WORKSHOP/ONLINE COURSE/CONFERENCE)

- **Mr.S.Senthil Rajan** attended **six days AICTE sponsored ATAL FDP** on **"Practical Insights into RF System Design"** organized by Marathwada Mitra Mandal's College of Engineering, Pune, Maharashtra from 06.01.2025 to 11.01.2025.

ATAL/2024/1735021904

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Nelson Mandela Marg, Vasant Kunj, New Delhi -110070

AICTE Training and Learning (ATAL) Academy

Certificate

It is certified that Mr. S SENTHIL RAJAN, Assistant Professor of Sri Venkateswara College of Engineering has successfully participated & completed AICTE Training And Learning (ATAL) Academy Faculty Development Program on Practical Insights into RF System Design at MARATHWADA MITRA MANDAL'S COLLEGE OF ENGINEERING from 06/01/2025 to 11/01/2025.

Anjali Bhatlawande Solanke
Associate Professor Level (AICTE Institute), Coordinator
MARATHWADA MITRA MANDAL'S COLLEGE OF ENGINEERING

Dr. Sunil Luthra
Director & Bureau Head
Training and Learning Bureau, AICTE

- **Dr.S.Vijayanand** attended **six days AICTE sponsored ATAL FDP** on **"Recent Trends in 5G/6G Wireless Communication"** organized by Department of Electronics and Communication Engineering, Samskruti College of Engineering and Technology, Hyderabad from 06.01.2025 to 11.01.2025.

ATAL/2024/1734617889

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AICTE Training and Learning (ATAL) Academy

Certificate

It is certified that Dr. S.Vijayanand, Assistant Professor of Sri Venkateswara College of Engineering has successfully participated & completed AICTE Training And Learning (ATAL) Academy Faculty Development Program on Recent trends in 5G/6G Wireless Communication at SAMSKRUTI COLLEGE OF ENGINEERING AND TECHNOLOGY from 06/01/2025 to 11/01/2025.

KannanVanisree
Associate Professor Level (AICTE Institute), Coordinator
SAMSKRUTI COLLEGE OF ENGINEERING AND TECHNOLOGY

Dr. Sunil Luthra
Director & Bureau Head
Training and Learning Bureau, AICTE

FACULTY PARTICIPATION

(SEMINAR/FDP/STTP/WORKSHOP/ONLINE COURSE/CONFERENCE)

- **Mr.P.Arul** attended an **one-week online Faculty Development Program (FDP)** on **"Mastering Research: Spotting Journal Scams & Finding Research Gaps",** organized by Promind Learning Academy, Erode, Tamilnadu from 13.01.2025 to 18.01.2025.

ProMind LEARNING ACADEMY

UDYAM-TN-07-0108200

PROMIND LEARNING ACADEMY

73/20 Veerappampalayam, Erode, Tamilnadu - 638 012, INDIA.

director@promindresearch.com, +91 94436 96035

CERTIFICATE OF PARTICIPATION

This is to certify that P. Arul from Sri Venkateswara College of Engineering has successfully completed the one-week online Faculty Development Program (FDP), "Mastering Research: Spotting Journal Scams & Finding Research Gaps" organized by ProMind Research Academy, Erode, from 13th to 18th January 2025.

DIRECTOR

Dr.S.Shankar M.E., Ph.D (IIT Madras)

Reference Number: PLA/2025/FDP-1/033

- **Dr.K.Bhuvaneshwari and Mrs.M.Stella Mercy** participated in **six days AICTE sponsored ATAL FDP** on **"AI-driven Innovations: Transforming Core Engineering Disciplines"** organized by SSN College of Engineering, Chennai from 20.01.2025 to 25.01.2025

ATAL/2024/1732772414

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AICTE Training and Learning (ATAL) Academy

Certificate

It is certified that ***Mrs. STELLA MERCY M, Assistant Professor*** *of* ***Sri Venkateswara College of Engineering*** *has successfully participated & completed AICTE Training And Learning (ATAL) Academy Faculty Development Program on* ***AI-driven Innovations: Transforming Core Engineering Disciplines*** *at* ***SRI SIVASUBRMANIYA NADAR COLLEGE OF ENGINEERING*** *from* ***20/01/2025*** *to* ***25/01/2025.***

Nalinkanth V Ghone
Associate Professor Level (AICTE Institute), Coordinator
SRI SIVASUBRMANIYA NADAR COLLEGE OF ENGINEERING

Dr. Sunil Luthra
Director & Bureau Head
Training and Learning Bureau, AICTE

FACULTY PARTICIPATION

(SEMINAR/FDP/STTP/WORKSHOP/ONLINE COURSE/CONFERENCE)

- **Dr.G.Ayappan** attended in **six days AICTE sponsored ATAL FDP** on **"Artificial Intelligence Techniques in VLSI Design"** organized by PSNA College of Engineering and Technology, Dindigul from 20.01.2025 to 25.01.2025

ATAL/2025/1737005961

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Nelson Mandela Marg, Vasant Kunj, New Delhi -110070

AICTE Training and Learning (ATAL) Academy

Certificate

It is certified that ***Dr. G AYAPPAN, Assistant Professor*** *of* ***Sri Venkateswara College of Engineering*** *has successfully participated & completed AICTE Training And Learning (ATAL) Academy Faculty Development Program on* ***Artificial Intelligence Techniques in VLSI Design*** *at* ***PSNA COLLEGE OF ENGINEERING AND TECHNOLOGY , DINDIGUL*** *from* ***20/01/2025*** *to* ***25/01/2025.***

G Athisha
Professor Level (AICTE Institute), Coordinator
PSNA COLLEGE OF ENGINEERING AND TECHNOLOGY , DINDIGUL

Dr. Sunil Luthra
Director & Bureau Head
Training and Learning Bureau, AICTE

FACULTY PUBLICATION
(JOURNAL/CONFERENCE)

- **Mrs.B.Elakkiya** published the research paper titled **"GradTX Net: Leveraging Transformers for Accurate Diabetic Foot Ulcer Severity Grading"** in Nineth **International Conference on Information System Design & Intelligent Applications (ISDIA 2025)** held at **University of Wollongong in Dubai (UOWD)** in association with **Hive Pro, Dubai** from 03.01.2025 to 04.01.2025
- **Mrs.B.Elakkiya** published the research paper titled **"CDR-CNN: Convolutional Neural Networks for Alzheimer's Disease Severity Prediction with Clinical Dementia Rating"** in **IEEE Xplore.**
- **Mrs.S.M.Mehzabeen and Dr.R.Gayathri** published the research paper titled **"Heuristically Improvised rice disease classification framework based on adaptive segmentation with the fusion of LSTM layer into Multi-Scale Residual attention Network"** in **Biomedical signal processing and control.**
- **Mr.N.Sathish** published the research paper titled **"Optimized Distance Vector Hop Localization Based on Pelican Optimization Algorithm in Underwater Wireless Sensor Networks"** in **International Journal of Communication Systems.**
- **Dr.G.Ayappan** published the research paper titled **"Automatic detection and prediction of COVID-19 in cough audio signals using the Coronavirus Herd Immunity Optimizer Algorithm"** in **Scientific Reports.**

FACULTY PROPOSAL SUBMISSION

(APPLIED/GRANTED)

- **Dr.R.Gayathri, Dr.A.Ramya, Mrs.S.M.Mehzabeen and Mrs.S.Mary Cynthia** were received **BIS Project fund, Rs.5,25,000** for the project titled **"Study of Lightning accidents and Early warning systems in India to assess Lightning Safety Measures"**

Sri Venkateswara College of Engineering

Autonomous Institution - Affiliated to Anna University
Pennalur, Sriperumbudur, Tamil Nadu | www.svce.ac.in

CERTIFICATE OF APPRECIATION

The Management of Sri Venkateswara College of Engineering, Pennalur, Sriperumbudur, would like to

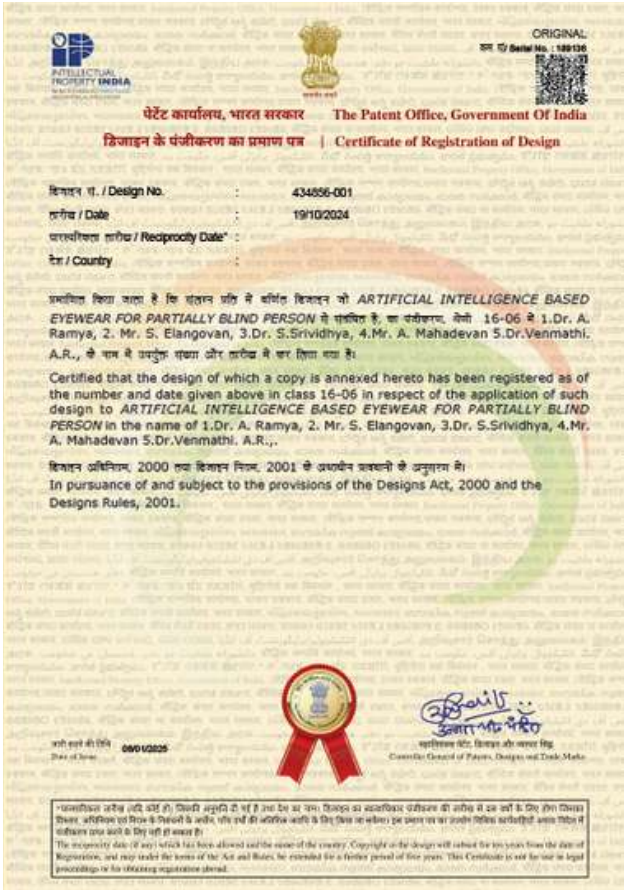
Congratulate ~~Mr/Mr./Prof~~ S.M. Mehzabeen Designation Assistant Professor

working in the Department of Electronics and Communication Engg. for ~~his/her~~ contribution on receiving a Grant / ~~Publication~~ of Design ~~/ Book Chapter~~ / Patent Titled AI based Nerve actimtion device for Healthcare Treatment, Application No. 433205-001 filed on 8/10/2024 and granted on 2/12/24

DEAN (RESEARCH) PRINCIPAL

PATENT GRANTED

- **Dr.A.Ramya, Mr.S.Elangovan, Dr.S.Srividhya, Mr.A.Mahadevan Dr. A.R.Venmathi** published a design patent titled, **"Artificial Intelligence Based Eyewear for partially blind person"** (Patent No. 434856-001) on 06.01.2025



ORIGINAL

पेटेंट कार्यालय, भारत सरकार The Patent Office, Government Of India

डिजाइन के पंजीकरण का प्रमाण पत्र | Certificate of Registration of Design

डिजाइन सं. / Design No. : 434856-001

फाइलिंग / Date : 19/10/2024

पारस्परिक तारीख / Reciprocity Date* :

देश / Country :

प्रमाणित किया जाता है कि संलग्न प्रति में वर्णित डिजाइन जो *ARTIFICIAL INTELLIGENCE BASED EYEWEAR FOR PARTIALLY BLIND PERSON* से संबंधित है, का पंजीकरण, वर्ग 16-06 में 1.Dr. A. Ramya, 2. Mr. S. Elangovan, 3.Dr. S.Srividhya, 4.Mr. A. Mahadevan 5.Dr.Venmathi. A.R., के नाम से उपर्युक्त संख्या और तारीख से कर लिया गया है।

Certified that the design of which a copy is annexed hereto has been registered as of the number and date given above in class 16-06 in respect of the application of such design to *ARTIFICIAL INTELLIGENCE BASED EYEWEAR FOR PARTIALLY BLIND PERSON* in the name of 1.Dr. A. Ramya, 2. Mr. S. Elangovan, 3.Dr. S.Srividhya, 4.Mr. A. Mahadevan 5.Dr.Venmathi. A.R.,.

डिजाइन अधिनियम, 2000 तथा डिजाइन नियम, 2001 के उपबंधों तथा अनुसरण में।
In pursuance of and subject to the provisions of the Designs Act, 2000 and the Designs Rules, 2001.

Date of Issue 06/01/2025

Controller General of Patents, Designs and Trade Marks

FACULTY ACHIEVEMENTS

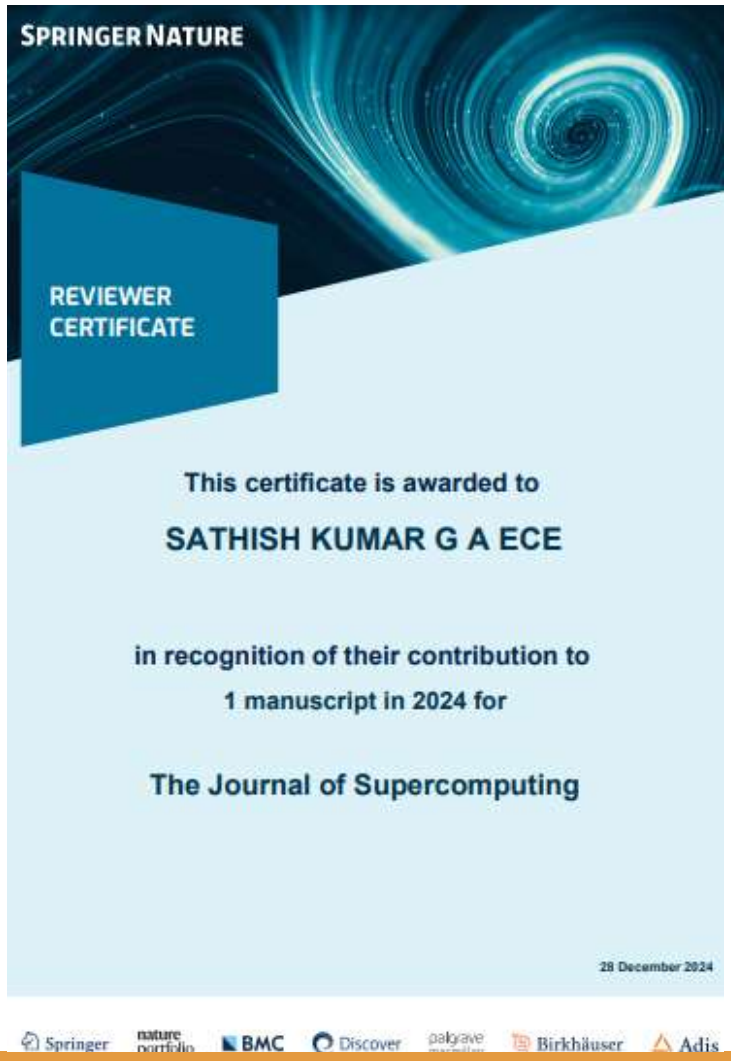
- **Mrs.S.Radhika** successfully **defended her Ph.D Viva-voce Examination** on the research topic of **"Certain Investigations on feature selection algorithm and Machine learning classifier for effective speech emotion recognition"** under the guidance of **Dr.S.Ramya (Research Coordinator)** organized by Department of Electronics and Communication Engineering held at **Sri Venkateswara College of Engineering (Autonomous), Sriperumbudur** on 10.01.2025

- **Mr.A.G.Murali Krishna** received **appreciation** for serving as a **reviewer** for third IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation **(IATMSI-2025)** organized by **IEEE MP Section and ABV-IIITM Gwalior, India.**

FACULTY ACHIEVEMENTS

- **Mrs.K.Bhuvaneshwari** successfully **defended her Ph.D Viva-voce Examination** on the research topic of **"Design and Analysis of laser-free nano-scale 2D Multipurpose photonic crystal biosensors"** organized by Department of Electronics and Communication Engineering held at **IFET College of Engineering (Autonomous), Villupuram** on 28.01.2025

- **Dr.G.A.Sathish Kumar** received **reviewer certificate** for reviewing the manuscript in **Springer Nature (The Journal of Supercomputing)**



REPUBLIC DAY CELEBRATION

- **Dr.G.A.Sathish Kumar** acted as a **chief guest** by hoisting the flag and delivered the importance of republic day to the students and faculty members on 26.01.2025

STUDENT PARTICIPATION

(Co-curricular Activities/Extra-curricular Activities)

- **Mr.S.Lohith Ashwa (II Year ECE)** participated in the event of **"NAF's Uzhavu Hackathon"** organized by Indian Institute of Technology, Madras on 05.01.2025

- **Mr.S.Lohith Ashwa (II Year ECE)** participated in the event of **"ROBOSCOCCER"** organized by Indian Institute of Technology, Madras on 06.01.2025

- **Ms.V.Sophia and Ms.R.Shrivani (II Year ECE)** participated in **YRC-MEGA AWARENESS PROGRAMME 2025 on the topic of "Road Safety Awareness"** organized by Sri Venkateswara College of Engineering (Autonomous), Sriperumbudur on 23.01.2025

Sri Venkateswara College of Engineering

23/01/2025 Certificate. No: 2025/YRC/04/ECE/176

ATTENDANCE CERTIFICATE

This is to certify that **SOPHIA V** has attended the YRC-Mega Awareness Programme 2025 - Talk on Road Safety Awareness, organized by Youth Red Cross, SVCE held at Sri Venkateswara College of Engineering, Pennalur, Sriperumbudur Tk on 23rd January, 2025. This certificate is issued for the purpose of Personality and Character Development (PCD) programme participation record under Clause 4.2 of UG Regulation 2022.

Student's Register Number	Branch of Study	Year	Section	Hours accounted for
2127230701139	ECE	II	C	8

Dr. R. Govindaraasu
YRC Coordinator

Sri Venkateswara College of Engineering

23/01/2025 Certificate. No: 2025/YRC/04/ECE/163

ATTENDANCE CERTIFICATE

This is to certify that **Shivani R** has attended the YRC-Mega Awareness Programme 2025 - Talk on Road Safety Awareness, organized by Youth Red Cross, SVCE held at Sri Venkateswara College of Engineering, Pennalur, Sriperumbudur Tk on 23rd January, 2025. This certificate is issued for the purpose of Personality and Character Development (PCD) programme participation record under Clause 4.2 of UG Regulation 2022.

Student's Register Number	Branch of Study	Year	Section	Hours accounted for
2127230701134	ECE	II	C	8

Dr. R. Govindaraasu
YRC Coordinator

STUDENT AWARDS

- **Ms.M.Sakthi Maheswari** was awarded the title of **"College Topper"** across all departments in the 2020-24 batch with an impressive **CGPA of 9.85.**
- **Ms.M.Srivani** secured **third rank** across all departments in the 2020-24 batch with an impressive **CGPA of 9.7**

- **Ms.M.Sakthi Maheswari (Batch 2020-24)** secured the **first rank** and awarded a **gold medal (Top performer)** in the Department of Electronics and Communication Engineering held in graduation day'2025 on 25.01.2025
- **Ms.M.Srivani (Batch 2020-24)** secured the **third rank** and awarded a **silver medal (Top performer)** in the Department of Electronics and Communication Engineering held in graduation day'2025 on 25.01.2025

INTERNSHIP TRAINING

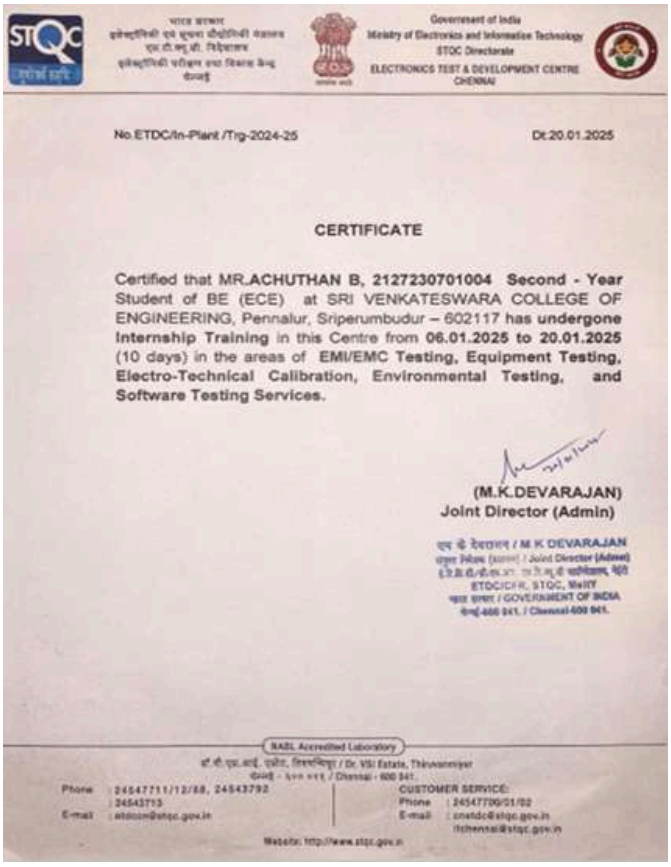
- Around **48 Students** completed the internship during the **last semester** in various government and private organizations such as **BSNL, CMRL, Southern Railways, ERNET, Electronic Testing and Development Centre, HCL Technologies, Lenovo, Flextronics Technologies etc.**

BHARAT SANCHAR NIGAM LIMITED
(A GOVERNMENT OF INDIA ENTERPRISE)
TRICHY TELECOM DISTRICT
BSNLearning
CERTIFICATE

This is to certify that Selvi. VARSHA.P (2127220701154), a student of III year B.E (ECE), Sri Venkateswara College of Engineering, Sriperumbudur- 602117 undergone Internship Training on "Telecom Technologies" in our organization for a period of 2 weeks from 18.12.2024 and completed the training successfully.

30/12/24
सहायक महाप्रबंधक (प्रशा/एचआर)
Assistant General Manager (Admn.& HR)
कार्या.प्रमप्र. एस.एन.एल.तिरुचि
O/o GM, BSNL, Trichy – 620 001

Place: Trichy
Date : 30.12.2024



STQC
Government of India
Ministry of Electronics and Information Technology
STQC Directorate
ELECTRONICS TEST & DEVELOPMENT CENTRE
CHENNAI

No.ETDC/In-Plant /Trg-2024-25 Dt.20.01.2025

CERTIFICATE

Certified that MR.ACHUTHAN B, 2127230701004 Second - Year Student of BE (ECE) at SRI VENKATESWARA COLLEGE OF ENGINEERING, Pennalur, Sriperumbudur – 602117 has undergone Internship Training in this Centre from 06.01.2025 to 20.01.2025 (10 days) in the areas of EMI/EMC Testing, Equipment Testing, Electro-Technical Calibration, Environmental Testing, and Software Testing Services.

(M.K.DEVARAJAN)
Joint Director (Admn)
एम के देवराजन / M K DEVARAJAN
ETDC/CFR, STQC, MeitY
GOVERNMENT OF INDIA

NABL Accredited Laboratory
Phone : 24547711/12/88, 24543792
E-mail : etdcom@stqc.gov.in
CUSTOMER SERVICE:
Phone : 24547700/01/02
E-mail : cnetdc@stqc.gov.in
Website: http://www.stqc.gov.in

HCLTech
hcltech.com

INTERNSHIP COMPLETION CERTIFICATE

11-07-2024

This is to certify that **Mr M. Vijay Viswanath,** a third-year B.E ECE student at Sri Venkateswara College of Engineering for completing an internship in Chatbot using Python **at HCL Technologies**. The internship lasted four weeks, from June 12th to July 11th, 2024

During the course of the internship, he has exhibited an enthusiastic attitude toward learning. We found the candidate to be highly self-motivated and hard-working. In addition to his work on Chatbot, he also gained valuable knowledge in embedded systems.

We are extremely satisfied with the candidate's performance and wish them great success in their future endeavors.

Regards,

SNEGAA J S
SENIOR SOFTWARE ENGINEER

HCL TECHNOLOGIES LIMITED
AMB - 5
CHENNAI
600 058

HCL Technologies Ltd.
Registered Office
HCL

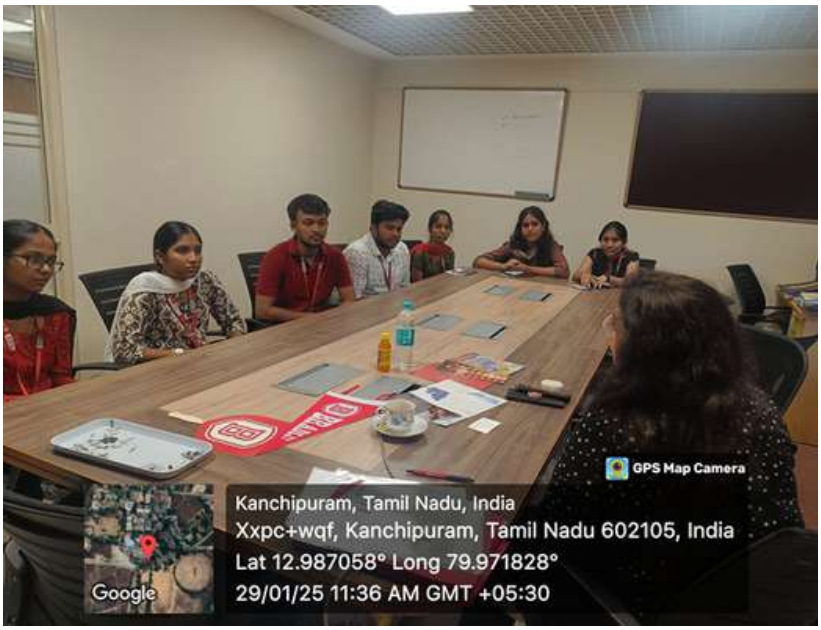
PLACEMENT ACTIVITIES

- **Final year students** attended the **Core Technical Training Program** for competitive exams and placement drives organized by the department of ECE from 02.01.2025 to 08.01.2025

- **Third year students** attended the **Technical Training Program** organised by placement cell from 02.01.2025 to 10.01.2025.

HIGHER STUDIES PROGRAM

- **Third and Final year students** attended the **"Overseas Education Fair"** organized by training and placement cell held at SVCE placement office on 29.01.2025



BIS ACTIVITIES

- **Ms.L.Ashika (II Year ECE)** secured **third prize** in **Poster Contest and Standards Writing Contest** on the theme of **"Decoding Product Standards: A Consumer's Roadmap to Quality"** organized by **Standards Club SVCE** in collaboration with the Bureau of Indian Standards (BIS)

ALUMNI ACTIVITIES

- The **Department of Electronics and Communication Engineering** organized a **guest lecture** on the topic of **"Trends in Server Architecture for Running AI Workloads and Developments in Interconnect Technologies"** by **Adithya Muralidharan, Senior Staff Engineer at Intel Corporation, California, USA** (SVCE ECE Batch 2007-2011) on 24.01.2025 at 01.30 PM in the Function hall. His lecture was about the advancements in Ethernet and PCIe (Peripheral Component Interconnect Express) technologies which are crucial in optimizing data transfer speeds and enhancing system performance. He emphasized the significance of these technologies in the efficient running of AI workloads offering a practical understanding of their impact on server architecture. The event is coordinated by **Dr.D.Menaka and Mrs.S.Kalyani (Alumni Association Coordinators)**

ALUMNI ACHIEVEMENTS

- **Adithya Muralidharan, as a Senior Staff Applications Engineer at Intel Corporation, California, USA** has demonstrated a remarkable array of achievements that highlight his leadership and expertise in the tech industry. His impact is evident through his multifaceted contributions, which span from high-profile speaking engagements to fostering innovation and mentoring the next generation of engineers.

- **At the prestigious UMAGINE TN 2025,** a government-organized tech conference in Tamil Nadu, Adithya captivated the audience with his talk on the latest trends in the hardware industry, particularly focusing on semiconductors and AI advancements. His presentation highlighted the critical role of technology, showcasing his deep understanding of the sector and its future potential. His ability to articulate complex technological advancements made him a key figure at the event. Additionally, Adithya served as a **jury member** for the startup pitching contest organized by **Tamil Nadu Technology Hub (iTNT) Innovation Hub** focused on deep tech and AI, further showcasing his commitment to nurturing innovation and supporting emerging talents in the tech sector.
- **Adithya's influence extended to the global stage as a panelist at FiTen (FeTNA International Tamil Entrepreneur Network) 2025,** held in Madurai. As part of a distinguished panel, he contributed to a discussion on AI in healthcare, emphasizing hardware innovations that revolutionized this industry. His ability to bridge technology and societal impact underscored his vision for a healthier, smarter future. This event, gathering visionaries and innovators, underscored Adithya's versatility and his ability to address diverse tech sectors with authority.

ALUMNI TESTIMONIAL

Mr.Adithya Muralidharan,
Senior Staff Engineer,
Intel Corporation,
California, USA.

“At Sri Venkateswara College of Engineering, I found the ideal platform to cultivate my skills and career aspirations. The rigorous education and innovative opportunities provided laid a solid foundation for my professional journey. Our supportive community and inspiring professors empowered me to excel. Today, I attribute my success to the college's transformative influence, guiding me to achieve my goals with confidence and excellence”**-Mr.Adithya Muralidharan, (Batch 2007-2011)**

PROGRAM OUTCOMES

PO1: Engineering Knowledge: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PROGRAM OUTCOMES

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PROGRAM OUTCOMES

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: Create value to organizations as an EMPLOYEE at various levels, by improving the systems and processes using appropriate methods and tools learnt from the programme.

PEO2: Run an organization successfully with good social responsibility as an ENTREPRENEUR, making use of the knowledge and skills acquired from the programme.

PEO3: Contribute to the future by fostering research in the chosen area as an ERUDITE SCHOLAR, based on the motivation derived from the programme.

PROGRAM SPECIFIC OUTCOMES

PSO-1: An ability to apply the concepts of Electronics, Communications, Signal processing, VLSI, Control systems etc., in the design and implementation of application oriented engineering systems.

PSO-2: An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical and managerial skills to arrive appropriate solutions, either independently or in team.

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PROGRAM OFFERED BY THE DEPARTMENT

- **B.E. in Electronics and Communication Engineering**
- **M.E. in Communication Systems**
- **Ph.D / MS (by Research)**

EDITORIAL BOARD

CHIEF EDITOR

CO-EDITORS

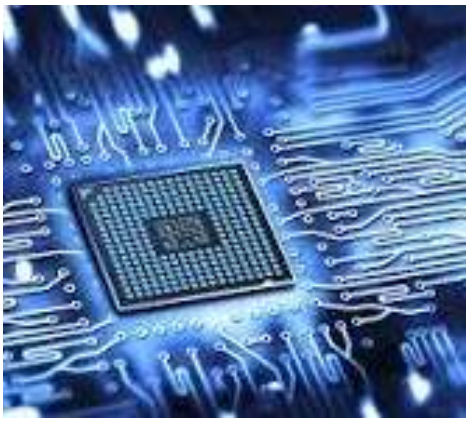
Sri Venkateswara College of Engineering

Autonomous Institution, Affiliated to Anna University, Chennai
Approved by the AICTE, Accredited by NAAC

ELECTRONICS AND COMMUNICATION ENGINEERING

ABOUT THE DEPARTMENT

The Department of ECE was started in the year 1985 and is presently accredited by the NBA. The postgraduate program (M.E) in Communication Systems was started in 2002. There are about 38 faculty members in the department and 14 of them are doctorates. The department is well equipped with lab facilities and software tools like IE3D, ADS, CST Studio, Lab View, Tanner Tools, Cadence, MATLAB, and Prototype Machine.



SALIENT FEATURES OF ECE

- The Program has been accredited by the NBA since April 2002.
- Recognized by Anna University, Chennai as an approved research centre for Ph.D. and MS (by Research) with effect from May 2009.
- The major thrust areas of research are RF and Microwave Engineering, Wireless Networks, Network Security, VLSI, Cognitive Radio, Image & Signal Processing, Neural Networks & Soft Computing, Embedded Systems & IoT, Machine Learning, Nano Technology, Robotics, and Artificial Intelligence.
- The department is doing a good number of consultancy work in the field of PCB Prototyping and RF measurements using a Network Analyzer.
- On average over 75 companies visit our department for campus placements External Research grant of Rs 48.26 Lakhs received from ISRO and Cognizant Technology Solutions in the last five years for carrying out various projects.
- Students actively participate in research projects related to Wireless Communications, Networking, Embedded Systems & IoT, Virtual Reality, Robotics, Drones etc.
- Student Counselling Service at SVCE is committed one to promote the mental health and well-being of our students by providing accessible, quality mental health services.
- Student counsellors are available on campus for confidential counselling to all students.
- The department has signed over 12 MOUs with reputed companies to ensure the Industry Institute Interaction.
- Training programs are being conducted to enhance the employability skills of the students and also to achieve good placement in various Industries.

MESSAGE FROM HoD's DESK

The Department of ECE consistently does a commendable job in disseminating the latest knowledge and inviting specialists from diverse domains for discussions on the most recent advancement and trends besides conducting regular classes. We hope every student who visits our department has an engaging, motivating and positive experience. We consistently strive to ensure that instructors and other staff personnel possess the necessary abilities and knowledge to stimulate their students' intellectual curiosity, creativity and critical thinking. I hope you enjoy your time here and thoroughly use our amenities for promising career development

Dr. G.A. SATHISH KUMAR HoD/ECE

VISIT WWW.SVCE.AC.IN

Contact US

Sri Venkateswara College of Engineering
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Pennalur Village
Chennai - Bengaluru Highways
Sriperumbudur (off Chennai) Tk. - 602 117
Tamil Nadu, India

+91-44-27152000

admissionenquiry@svce.ac.in

SCAN & APPLY

CHOOSING SVCE: A PATHWAY TO SUCCESS AND GROWTH

- One of the prestigious and top ranked Autonomous engineering institution affiliated to Anna University, Chennai.
- Accredited by NAAC and NBA.
- Over 28 % of the alumni work abroad.
- Highest placement offers of Rs.25 LPA and 20 LPA in PayPal and Amazon.
- Highly qualified faculty and staff with an average experience of over 20 years.
- World class Laboratories to foster innovation and research.
- Alumni working in fortune 500 companies like Google, Microsoft, Facebook, Mercedes Benz, INTEL, etc.,
- State-of-the- art-campus with modern amenities in the industrial corridor of Chennai.

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A Bachelor's Degree in Electronics and Communication Engineering with expertise in one of the following specialization

HONOURS SPECIALIZATION

Wireless Communication Systems

VLSI

Antenna and Microwave Technology

Signal Processing and Data Science

IoT Systems and its Applications

Networking and Security

Our Recruiting Companies

accenture, amazon, Deloitte., Infosys, wipro, Ford, Cognizant, CATERPILLAR, SCHWING Stetter, FLSmidth, PayPal, verizon, SIEMENS, ASHOK LEYLAND, ABB, ThoughtWorks, Tech Mahindra, Atos Syntel, Capgemini, TCS 50, YAMAHA, TechnipFMC, HEXAWARE, freshworks, Informatica, vedanta, wood., SAINT-GOBAIN, HCL, HYUNDAI, Honeywell, TVS, flex., TEMENOS

Top Universities where our students are pursuing Higher Education

NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE, PennState Great Valley, THE UNIVERSITY OF MELBOURNE, WISCONSIN, UNSW AUSTRALIA, Northeastern University, UNIVERSITY OF MARYLAND

MINORS

Artificial Intelligence and Machine Learning and Machine Learning

Data Science and Analytics

Robotics

Semiconductors

Advanced Communications

Bio-medical Signal Processing

And Many More....

Sri Venkateswara College of Engineering

Autonomous Institution, Affiliated to Anna University, Chennai
Approved by the AICTE, Accredited by NAAC

DEPARTMENT OF ELECTRONICS AND COMMMUNICATION ENGINEERING

M.E COMMUNICATION SYSTEMS

ADMISSIONS OPEN FOR THE ACADEMIC YEAR 2024-25

SVCE started the Department of Electronics and Communication Engineering in the year 1985. The Department offers B.E. in Electronics and Communication Engineering and M.E. in Communication Systems. It is also approved as aResearch Centre in Ph.D and MS (by Research) programmes by Anna University, Chennai.

ABOUT SVCE

Sri Venkateswara College of Engineering (Autonomous) is a premier self-financing institution started in the year 1985. The college offers 10 B.E/B.Tech Programmes and 10 M.E/M.Tech Programmes in Engineering and Technology. The Programs are approved by AICTE and the college is affiliated to Anna University, Chennai. The college is also accredited by National Assessment and Accreditation Council (NAAC). Many programs are accredited by National Board of Accreditation (NBA). The college is also certified by ISO 9001:2015. The institution received the autonomous status in the year 2016. Our Vision is to be a leader in Higher Technical Education and Research by providing state-of-the-art facilities to transform the learners into global contributors and achievers.

ADMISSION INFORMATION

A pass in a recognized Bachelor's degree or equivalent in the relevant field and should have obtained atleast 50% in the qualifying degree examination. Admissions are through Tamil Nadu Common Entrance Test (TANCET) conducted by Anna University or GATE

RESEARCH GRANTS

Our faculty members have received major external research grants from prestigious organizations such as ISRO, AICTE, DRDO, and TNSCST, etc., to the tune of ₹56.26 Lakhs in the last three years for doing various funded projects.

SCHOLARSHIPS FOR PG STUDENTS

- Tution fee (Rs. 50,000/year) waiver for 30% of the students of sanctioned class strength on merit basis, as applicable.
- Management Scholarship for tution fees and assistance for books and instruments.
- GATE Scholarship of Rs. 12,400 per month for students having valid GATE Score. Sponsorships for students to attend conferences.
- Intramural M.E/M.Tech Student Research Grant to carry out innovative projects.

RESEARCH AREAS

Join the Revolution: Transform Communication Systems with SVCE

- Biomedical Instrumentation
- Computer Networks & Network Security
- Digital Signal Processing & Image Processing
- Embedded Systems
- Fiber Optic Communication
- IoT (Internet of Things)
- Nano Electronics
- RF & Microwave Engineering
- Robotics & Artificial Intelligence
- VLSI & Microelectronics
- Wireless Communication Networks

MAJOR RECRUITERS

ERICSSON, CSS CORP, TAFE, amazon, TATA COMMUNICATIONS, ZOHO Work. Online, Infosys, Cognizant, WIPRO, accenture High performance. Delivered., L&T Infotech, HCL