



SRI VENKATESWARA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
&
ELECTRONICS AND COMMUNICATION ENGINEERS ASSOCIATION
&
THE INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS-SF
&
ROBOTICS AND ARTIFICIAL INTELLIGENCE CLUB

REPORT ON GUEST LECTURE ON VLSI

The guest lecture on VLSI was organised and coordinated by the Electronics and Communication Engineers Association (ECEA), along with Institution of Electronics and Telecommunication Engineers (IETE) - Student Forum, and the Robotics and Artificial Intelligence Club (RAIC) of Sri Venkateswara College of Engineering, on Tuesday, 7th March 2023, in the college premises. The Chief Guest & the expert key speaker of this event is Dr. K. Saravanan – Design Engineer, Physical Design, Cerium system.

This guest lecture was conducted exclusively for pre-final year students belonging to the department of ECE. The venue of the Guest Lecture was classroom no. 506. The motive of the Guest Lecture was to improve the knowledge on VLSI for the students & provide instincts in the current technological trends in the field.

Commencement of the event	7 th March, 2023 (9:30 AM IST)
End of the event	7 th March, 2023 (12:00 PM IST)
Total Participants	100 Participants

PROPOSAL OF THE EVENT



Sri Venkateswara
College of
Engineering



RAIC

SRI VENKATESWARA COLLEGE OF ENGINEERING Pennalur, Sriperumbudur Taluk -602117

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

In Association with

ELECTRONICS AND COMMUNICATION ENGINEERS' ASSOCIATION – SVCE

&

INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS-SF

&

ROBOTICS & ARTIFICIAL INTELLIGENCE CLUB

Proposal for conducting "Guest Lecture on VLSI"

ECE Association, IETE - Students Forum and RAIC of SVCE is planning to conduct a "Guest Lecture on VLSI" on Tuesday, 7th March 2023 in our college premises. The guest lecture is conducted exclusively for III year students.

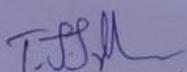
The chief guest and the expert key speaker of this guest lecture is Dr.K. Saravanan, Design Engineer, Physical Design, Cerium system with 2.5 years of hands-on experience in VLSI design.

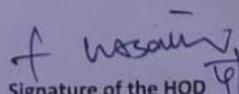
This event is aimed to improve the student's knowledge on Verilog coding, future trends of VLSI and also to provide instincts on the current technological trend. Kindly approve this proposal and grant permission to conduct this guest lecture.

Venue: III Year Classroom

Timing: 9:30 A.M onwards

Thank You


Signature of the Faculty Co-ordinator


Signature of the HOD 4/3/23

AGENDA OF THE EVENT



SvCE Sri Venkateswara
College of
Engineering

RAIC



SRI VENKATESWARA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION
ENGINEERING
along with
ELECTRONICS AND COMMUNICATION ENGINEERS ASSOCIATION
&
THE INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS -
STUDENTS FORUM

Solicits your esteemed presence for the

GUEST LECTURE (2022-2023)



Dr.Saravanan.K

Design Engineer
Cerium Systems
Bengaluru

DATE :07.03.2023

TIME : 09.30 AM

VENUE : V-BLOCK-506



AGENDA

9:35 AM-9:40 AM - **Introduction of the Chief Guest by
Dr. T.J. Jeyaprabha – ECEA, IETE SF, RAIC,
FODSE Co-ordinator**

9:40 AM-11:50 AM - **Technical Talk on “VLSI Physical Design”**

11:50 AM-12:00 PM - **Vote of Thanks by Mr. Athappan M,
Associate Professor, Dept. of ECE SVCE**

About the guest:

The guest lecture was delivered by Dr. K. Saravanan – Design Engineer, Physical Design, Cerium system. He completed his education at Vel Tech Engineering College in VLSI Design. He has 15+ years' experience of teaching & working in the designing & fabrication of VLSI. His vast knowledge in the design technologies has proved to have inspired the students to develop an interest in VLSI from a career and academic perspective.

About the event:

The session commenced with Dr. T.J. Jeyaprabha, Associate Professor – Department of ECE welcoming the guest lecturer Mr. Saravanan K. It was followed by a detailed lecture on the basics of the fabrication process of chips by the Guest Speaker. The students were introduced to a solid briefing about the basics of Logic Gates & CMOS circuits. The application of concepts & application through simulation, verification, and physical implementation of chips. He further explained about the process of optimization in the chip manufacturing industries.

The speaker briefed the participants about the latest developments in the domain of VLSI, its significance in the current world, and how it can emerge as a field of opportunities for engineers. He spoke about his role as a Design Engineer, and he gave an overview about the products and devices that are manufactured. He also designed and described different adder architectures & data path circuits such as comparators & shifters. The Speaker stressed the importance of design thinking principles in the domain. He also spoke about the various errors that can occur in the process and the several consequences of the same through case studies.

Salient features of the Guest Lecture :

- Importance of VLSI design in the current world scenario.
- Solid introductory knowledge on VLSI concepts using standard introductory tools.
- Widespread usage of tools like Cadence in the industry.
- Importance of Testing and Quality Assurance department in this field.
- Top Companies hiring candidates proficient in VLSI domain.

The session was truly interesting and enlightening. All the participants were inspired by the knowledge portrayed by the chief guest speaker. The chief guest speaker was also very interactive and answered every question put forth by the participants during the “Q&A” session.

The session concluded with a Vote of Thanks by Mr. Athappan M, Associate Professor, Department of ECE. He appreciated the enlightening knowledge transfer & the efforts of the organizing committee. The event received an overall positive response & enthusiasm from the participants & faculty.

Some snaps from the session:

Snapshot of the event commencement



Snapshot of Honouring the Chief Guest



Participants List of the event:

SR No	REGISTER NUMBER	NAME	SIGN
1	2127200701022	Ashratha . M . R	
2	2127200701049	Hosibha . V . L	V.L. Hosibha
3	2127200701006	ABINAYA . G	Abinaya G
4	2127200701029	DHANA SRI . R	
5	2127200701015	ANIRUDH . R	
6	2127200701016	R . APARNA	
7	2127200701003	AARTHI . S	
8	2127200701009	Adithya . V	
9	2127200701012	AKSHAY KUMAR . S	
10	2127200701001	Aadithya Prasad	
11	2127200701014	Ambirish . Y	
12	2127200701047	Hemanti Kumar . V	
13	2127200701044	Harshan . T . S .	
14	2127200701021	Arvindh G	
15	2127200701026	Bharathi . H .	
16	2127200701045	HARSHAVARDHAN	
17	2127200701041	HARSHAN . G	
18	2127200701037	Ganuvijay . H	
19	2127200701035	Ganapriyath . S	
20	2127200701036	Gokul . F	
21	2127200701029	Bella Tirupati Naidu	
22	2127200701020	ARJUN VIJAY	
23	2127200701008	Adithya . N	

1023

ECE - B (III year)
GUEST LECTURE ON VLSI PRODUCT DESIGN

REGISTER NUMBER	NAME	SIGN
2127200701311	Santhosh Kumar P	Santhosh
2127200701096	Prasanna Kumar R	Prasanna
2127200701098	Preetham Raj MB	Preetham
2127200701087	Navan Kumar . S	Navan Kumar S
2127200701061	Keerthana . R	Keerthana
2127200701064	Kaithika Shree . D	Kaithika
2127200701074	Manoon Bin Fashila . M	Fashila
2127200701070	G. Madhumitha	G. Madhu
2127200701066	Lakshana . S	Lakshana
2127200701068	Lokesh . A	Lokesh
2127200701052	K.L. Jeevanesh	K.L. Jeevanesh
2127200701057	Karthikeyan . V	Karthikeyan V
2127200701059	Karla Varsha . P.B	Varsha

ECE C-SEL [III YEAR] GUEST LECTURE ON VLSI PRODUCTION

REG NO	NAME	SIGNATURE
200701130	SAIMYASA VENKATAN	mi det
2 200701139	R. Uma Maheswari	
3 2007 01133	S. Sairashmi	S. Sairashmi
4 200701112	Sai Shakti.S	
5 200701129	SR Rekha.T	
6 200701108	M. RAJA	
7 200701134	Subbin Sundramy	
8 200701 2 2	sashidhar . G	
9 2007 01142	Vasanth . P	Vasanth P
10 20070 1147	Vishnu Prabhath C.M	
11 20070 1144	Vijay K	
12 200701121	Sarvesh Kumar V	
13 2004 0113	K. Sai Sundar	
14 200701317	S. Vignesh	
20070 1116	Sakthiprasad L	
16 200701100	Pochishi . S	
17 200701120	Sowesh R . S.	
18 200701143	P. Vignesh	
19 200701128	Sreevatsav. E	
20 200701315	Sudharsanar. J	
21 200701149	V. Yashith	
22 200701145	S. Vijayarathiy	
23 20070 1119	BANHASHI KUMAR . S	

Organizing teams:

ECEA Comprising of:

President	: Mr. Gugesesh R (IV Year ECE A)
Vice-President	: Mr. Sangeeth Kanna P (IV Year ECE C)
Secretary	: Mr. V.S.Prithiviraj (III Year ECE C)
Treasurer	: Ms. Sahana Balasubramaniam (III Year ECE C)
Executive Members	: Mr. Aakash (III Year ECE A) : Mr. Ganeshan H (III Year ECE A) : Mr. Pratosh Karthikeyan (III Year ECE B) : Mr. Pranav A (III Year ECE B) : Mr. Raswanth U (III Year ECE C) : Mr. Sowndhar R (III Year ECE C)
Joint Secretary	: Ms. Dharani A (II Year ECE A) : Mr. Parvesh R (II Year ECE B) : Mr. Umesh Anandh S (II Year ECE C)

IETE SF SVCE comprising of:

Chairman	: Mr. Sivasubramanian R
Vice Chairman	: Mr. Deepak Akash Raj T
Honorary Secretary	: Ms. Mrdulla V Naarayan (III Year ECE B)
Honorary Treasurer	: Ms. Lakshana Sasikumar (III Year ECE B)
Executive Members	: Mr. Arvindh G (III Year ECE A) : Mr. Avinash P (III Year ECE A) : Mr. Nirmal Kumar T K (III Year ECE B) : Mr. Nithish P (III Year ECE B) : Ms. Sakthi Maheswari M (III Year ECE C) : Mr. Shashidar G (III Year ECE)
Joint Secretary	: Mr. Ashish S (II Year ECE A) : Ms. Nivetha D R (II Year ECE B) : Mr. Tharun K R (II Year ECE C)

AIC Comprising of:

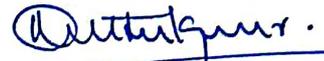
President	:Ms. Krishna Priya S (IV Year ECE B)
Vice-President	:Mr.Hari Prasad P (IV Year ECE A)
Secretary	:Mr.Sanjay Lokesh A M (III Year ECE C)
Joint Secretary	: Mr.Anish Krishnan (II Year ECE A)
	: Mr.Mahith I K (II Year ECE B)
	: Mr.Sharad L (II Year ECE C)
Mentors	:Mr. TRHari Prasanna (IV Year ECE A)
	: Mr.MKishore (IV Year ECE B)
	: Ms. Subashree (IV Year ECE C)
	:Mr.Ganeshan H (III Year ECE A)
	: Mr.Magesh S (III Year ECE B)
	: Mr.Rajeshvar M Swamy (III Year ECE C)
	: Ms. Snehalatha M (III Year ECE C)
	: Ms. Srivani M (III Year ECE C)
	: Ms. Vishnu Priya V T (III Year ECE C)



Dr.TJJeyaprabha
Associate Professor,ECE
ECEA, ISF,RAIC Coordinator



Mr. S Elangovan
Assistant Professor, ECE
ECEA, ISF,RAIC Coordinator



Dr.S Muthukumar
Professor & HOD-ECE

DATE:24/03/2023

REPORTBY:
Ms. S LAKSHANA
(Honorary Treasurer, IETE-SF,SVCE)