



SRI VENKATESWARA COLLEGE OF ENGINEERING

ALUMNI ASSOCIATION OF ELECTRONICS AND COMMUNICATION ENGINEERING

TRENDS IN VLSI DESIGN

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
ECE ALUMNI ASSOCIATION
PRESENTS

TRENDS IN VLSI DESIGN

A WEBINAR
BY

Mr. Suba Chandran N
ECE Alumnus -Batch of 2014
DFT Engineer, Intel Technology

ON

17/04/2021 | 5 PM - 6 PM

Registration Link : <https://forms.gle/DYxyRpnD5EPQUHw7>
Meet Link : <https://meet.google.com/chm-uzvb-pxf>

The ECE Alumni Association, organized –TRENDS IN VLSI DESIGN, a webinar on VLSI Design, for the academic year 2020 - 2021 on 17th April, 2021 via Google meet platform. Ms. Suwetha K , Treasurer, Alumni Association (ECE), SVCE, welcomed the gathering.

The Chief Guest, Mr. Suba Chandran N, began the session with a brief introduction about the trends in development of ICs in accordance with Moore's law.

The screenshot displays a Google Meet interface during a webinar. The main window shows a presentation slide titled "Moore's Law" with the following content:

- <https://www.youtube.com/watch?v=Hoqa-fBsQfs>
- Moore's Law is the prediction that the number of transistors in a dense integrated circuit doubles every two years as technological progress advances.
- The observation was made by Gordon Moore, co-founder of Intel, who saw that the size of transistors was shrinking rapidly due to continuous innovation.

The slide also includes a "meet.google.com is sharing your screen" notification and a "Stop sharing" button. The bottom of the slide shows a Windows taskbar with the time 5:03 PM on 17 Apr 21.

On the right side of the screen, a "People (7/8)" panel lists the participants in the call:

- Alumni Association (You)
- ADITHYAN TAWKER ECE
- ANUSHOBKA P.ECE
- ASWINE ECE
- BHADRATH KRISHNA A.J.
- DEEPIKA ECE
- DIYA RAJIV CHRISTOPH.
- GAVATHRI C
- GEETHAPRIYA N.ECE
- GUJANESH R.ECE
- haritha kumar saravan...
- HARISHKUMAR G K ECE
- HARITHA R.ECE
- HASHINI ECE
- HITHAISH U M ECE
- HOD ECE
- JAYIA LAKSHMIAN S ECE
- KALANJANAN M ECE

At the bottom of the screen, there are icons for "Turn on captions" and "suba chandran is presenting".

Then he gave a brief explanation about the Gate array and FPGA along with its fabrication process and VLSI Design flow. In addition to that he gave a clear insight on various testing procedures.

The screenshot displays a Google Meet interface. The main window shows a slide titled "VLSI Design Flow" with a flowchart. The flowchart starts with "Front End" (Design Specifications, Behavioral Description, RTL Description (HDL)) leading to "Functional Verification And Testing" and "Logic Synthesis". "Logic Synthesis" leads to "Logical Verification And Testing", which then leads to "Floor Planning and Automatic Place and Route", "Physical Layout", and finally "Layout Verification and Implementation" leading to "FAB". There are "Back Test" and "Test" labels on the flowchart. The right sidebar shows a list of 14 participants in a call, including names like SHAI NI ECE, YUKESH ADITHYAN ECE, MENAKA D ECE, KOUSAVYA R ECE, SHAI NI ECE, Ritulaa K, VIDYA M ECE, sankara narayanan, GANANESH R ECE, ADITHYAN TANNER ECE, ANUSHOBHA F ECE, ASHWINI ECE, BHARATH KRISHNA J..., DEEPIKA ECE, DEVI PRIYA ECE, DIVYA BHARATHI ECE, DIVYA RAJIV CHRISTOPH..., GAYATHRI C, GEETHAPRIYA ECE, GUGANESH R ECE, Harshita kumar saravin..., HARSHITHABAR G K ECE, HARITHA R ECE, HAGHINI ECE, HITHASHI U M ECE, and JAYIA LAKSHMANI ECE. The bottom of the screen shows the meeting controls and the presenter's name, subha chandran.

He went on to elaborate the importance of Functional verification and explained the design methodology which includes logic synthesis, logic verification etc., where the RTL is converted into a technology specific gate level net list which are then verified with a RTL description using STD cells.

Finally, the session was concluded with a Vote of Thanks by Mr. Guganesh R, Executive Member, Alumni Association, ECE, SVCE.

The screenshot shows a Google Meet interface. The main window displays a presentation slide titled "Test Flow" with a flowchart. The flowchart is divided into two main paths: one for "Masks" and one for "Packaged Device". The "Masks" path includes steps: Manufacturing, In-line Wafer Tests, Wafer Sort (GO/no-GO), DC Parameters, Functional, Logic, Delay, and Die. The "Packaged Device" path includes: Package Test, Burn-In, Package Test, Incoming Inspection, System Integration, System Test, and Customer. There are also "Test escapes" and "Fallout" points indicated. A credit line at the top of the slide reads: "Credit : <https://nptel.ac.in/content/storage2/courses/106103116/handout/mod7.pdf>". Another credit line at the bottom of the slide reads: "Credit : <http://ece-research.unm.edu/jimruis/test/supers/nim/overcpu1.htm>". The right side of the screen shows a list of participants: suba chandran, SHALINI ECE, Y, YAKESH ADITHYA ECE, RAJAWAN ECE, MENAKA D ECE, VIDYA M ECE, SARALA B Ece, and GUGANESH ECE. The bottom of the screen shows the meeting controls and the title "VLSI Design Workshop- ECE Alumni Association".

Participant Details:

Total Number of Participants: 82

There was an active and an enthusiastic participation of students from the ECE department of the college.

ALUMNI ASSOCIATION

(2020-2021)

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- | | | |
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| | RADHA G | (SECOND YEAR ECE B) |
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Mrs. D. MENAKA, AP, ECE

Mrs. M. VIDYA, AP, ECE

REPORT BY

GUGANESH R

II year, Executive member,
Alumni association, ECE, SVCE.

Webinar on " Trends in VLSI Design" on 17th April 2021

Attendance sheet

S.No	Participant Name
1	PARTHASARATHI T
2	POOJA M
3	POOJA R
4	PRABAKAR SK
5	PRABHU S S
6	PRATHIBHA SUSHMA N V
7	PRAVIN K.S
8	PREETHIKA S
9	PREMKUMAR R
10	PRIYA DARSHINI S
11	RAAJESH BAABU S
12	RAGHAVAN R
13	RAGHAVI S
14	RAHUL B
15	RAHUL NARAYANAN
16	RALLAPALLI UDAYASRI
17	RESHMI JAYARAJAN
18	RISHABANATH K
19	RISHI KUMAR R
20	SABARISH SUBRAMANIAM A.V
21	SAI SANTHOSH S
22	SAISARAVANAN P K
23	SANGEETHA R
24	SIVASAKTHI K
25	SOMESH P S
26	SANJANA B S
27	SANJAY PS
28	SARANYAA M
29	SATHAPPAN K
30	SATHYA B
31	SESHADRI N
32	SHABARISH HAREN V
33	SHAILESH KRISHNAN N
34	SHALINI A
35	SHIVAGANESHAN K
36	SHRIHARI S
37	SHRUTHI E
38	SIDDHARTH K
39	SIVASOORIYA M
40	SREEHARI S
41	SRI NATARAJ C
42	SRIHARI K

43	SRIMATHI S
44	SRIRAM R
45	SRIVANTH GANESH
46	SRIVARSHINI A
47	SUBASH KANNAN R K
48	SUBHA PRIYA A
49	SUDHARSAN K
50	SUDHARSANA S
51	SUSHMITHA S R
52	SUWETHA K
53	SWETHA S
54	SWETHA S
55	TAMIL SELVAN H
56	TEJASWATH R
57	THANIGAIVEL M
58	THIVYA T
59	UKKESH PB
60	VARUN SOMAN
61	VIDHYA N
62	VIGNESH M
63	VIGNESH T J
64	VIGNESHWAR S J
65	VIJAY BABU B
66	VIJAY MUTHU RAJA J
67	VIJAY SOORYA J
68	VINDHIYA S
69	VISHNUKUMAR Y
70	VISHNUSAI R
71	VISHNUVARADHAN M
72	VISHWESH P V
73	YASHWANTH B
74	YASHWIN VASANTH S
75	YOGESH G
76	YUKESH ADITIYA P S
77	VIGNESHWARA S
78	ANIRUDDH AIYENGAR
79	MAGESH S
80	MAHALAKSHMI M
81	JANANI A
82	JEEVAHARISH R



Co-ordinator



Hod-ECE



