SRI VENKATESWARA COLLEGE OF ENGINEERING
Department of Electronics and Communication Engineering

Submitted to The Principal requesting for Approval

Through HOD- EC

Date: 12-Feb-2019

The Department of ECE proposes to conduct **'5 Days Value Added Course on Hardware Modeling using Verilog HDL'** from **18-Feb-2019 to 22-Feb-2019** to approximately 30 numbers of Third Year Students of ECE Department, as part of the Academic Quality Improvement Program Plan (AQIPP) for the academic year 2018-19.

The schedule comprising of the topics covered and hands-on sessions are attached herewith for your kind perusal. The sessions will be handled by Dr.G.A.Sathish Kumar. Professor, Dr.S.R.Malathi, Associate Professor and Mr.M.Athappan Assistant Professor. A nominal fee of Rs.50/- per student will be collected towards Certificate Printing Charges.

We request you to kindly permit us to conduct the value added course and do the needful.

Thank you

12/2/19
Dr. S. R. Malathi
Co-ordinator

12/2/19.
Dr. S. Muthukumar
HOD-EC

To: HOD-EC
Approved
SC
13/2.

SRI VENKATESWARA COLLEGE OF ENGINEERING

Sriperumbudur- 602 117

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING
- RESEARCH CELL

Cordially invites you to the

5 Days Value Added Course on

'Hardware Modeling using Verilog HDL'

Conducted by

Dr.G.A.Sathish Kumar, Professor

Dr.S.R.Malathi, Associate Professor

Mr.M.Athappan, Assistant Professor

Ms. S. M. Mehzabeen, Assistant Professor

From 18-Feb-2019 to 22-Feb-2019

5 Days Value Added Course on Hardware Modeling using Verilog HDL
From 18-Feb-2019 to 22-2-2019
Schedule

Day & Session	Date, Time, Venue, Faculty	Topic
Day-1 Session-1	18.02.2019 08.30 a.m to 10.10 a.m 506 / 532 Dr.G.A.Sathish Kumar	A. Overview of Digital Design with Verilog HDL: 1. Evolution of Computer Aided Digital Design 2. Emergence of HDLs 3. Typical Design Flow 4. Importance of HDLs 5. Popularity of Verilog HDL 6. Trends in HDLs
Day-1 Session-2	18.02.2019 10.25 a.m - 12.05 p.m 506 / 532 Dr.G.A.Sathish Kumar	B. Hierarchical Modeling Concepts: 1. Design Methodologies. 2. Example: 4-bit Ripple Carry Counter 3. Modules, Instances, Components of a Simulation 4. Design Block, Stimulus Block, Example- Ripple Carry Counter C. Basic Concepts 1. Lexical Conventions 2. Data Types. 3. System Tasks and Compiler Directives
Day-1 Session-3	18.02.2019 12.45p.m - 03.15p.m 506 / 532 Mr. M.Athappan	D. Modules and Ports` 1. Modules- Components of Verilog Module. 2. Example: S-R Latch 3. Ports- List of ports – Port Declaration - Port Connection Rules- Connecting Ports to External Signals E. Gate-Level Modeling 1. Gate Types- AND/OR Gates, BUF/NOT Gates, 2. Array of instances, Examples: Gate-level multiplexer, 4- bit ripple carry full adder. Gate Delays- Rise, Fall, and Turn-off Delays, Min/Typ/Max Values, Delay Example
Day-2 Session-1	19.02.2019 08.30 a.m to 10.10 a.m 506 / 532 Mr. M.Athappan	F. Dataflow Modeling 1. Continuous Assignments, Delays. 2. Expressions, Operators, and Operands 3. Operator Types 4. Examples: 4-to-1 Multiplexer, 4-bit Full Adder, Ripple Counter
Day-2 Session-2	19.02.2019 10.25 a.m - 12.05 p.m 506 / 532 Dr. S.R.Malathi	G. Behavioral Modeling 1. Structured Procedures 2. Procedural Assignments 3. Conditional Statements 4. Multiway Branching, Loops 5. Sequential and Parallel Blocks 6. Examples: 4-to-1 Multiplexer, 4-bit Counter, Traffic Signal Controller –FSM design

Day-2 Session-3	19.02.2019 12.45p.m - 03.15p.m 506 / 532 Ms. S.M.Mehzabeen	H. Hands-on with FPGA - Research Scholar: Ms. Poomagazh
Day-3 Session-1	20.02.2019 08.30 a.m to 10.10 a.m 534 Dr. S.R.Malathi	I. Tasks and Functions 1. Functions - Function Declaration and Invocation. 2. Function Examples: Parity calculation, Left/right shifter. 7. Recursive Functions, Constant Functions, Signed Functions
Day-3 Session-2	20.02.2019 10.25 a.m - 12.05 p.m 534 Dr. S.R.Malathi	J. Switch-Level Modeling 1. Switch-Modeling Elements- MOS switches, CMOS switches. 2. Bi-directional switches, Power and Ground 3. Resistive Switches, Delay Specification on Switches. 4. Examples: CMOS Nor Gate, 2-to-1 Multiplexer, CMOS Inverter
Day-3 Session-3	20.02.2019 12.45p.m - 03.15p.m Ms. S.M.Mehzabeen	K. Hands-on with FPGA Research Scholar: Ms. Poomagazh Applied Electronic Lab
Day-4 Session-1	21.02.2019 08.30 a.m to 10.10 a.m Dr. S.R.Malathi	L. User-Defined Primitives 1. UDP basics, Combinational UDPs 2. Sequential UDPs, UDP Table Shorthand Symbols
Day-4 Session-2	21.02.2019 10.25 a.m - 12.05 p.m Ms. S.M.Mehzabeen	M. Hands-on with CADENCE software Tool Research Scholar: Ms. Poomagazh Applied Electronic Lab
Day-4 Session-3	21.02.2019 12.45p.m - 03.15p.m Ms. S.M.Mehzabeen	N. Hands-on with CADENCE software Tool Research Scholar: Ms. Poomagazh Applied Electronic Lab
Day-5 Session-1	21.02.2019 08.30 a.m to 10.10 a.m Ms. S.M.Mehzabeen	O. Hands-on with CADENCE software Tool Research Scholar: Ms. Poomagazh Applied Electronic Lab
Day-5 Session-2	21.02.2019 10.25 a.m - 12.05 p.m Ms. S.M.Mehzabeen	P. Hands-on with CADENCE software Tool Research Scholar: Ms. Poomagazh Applied Electronic Lab
Day-5 Session-3		Technical Talk by Chief Guest Certificate Distribution Valedictory

A Report of Value Added Course on "Hardware Modelling using Verilog HDL" Organized on 18th – 22nd Februaury 2019

The Five Days programme on "Hardware Modelling using Verilog HDL" is held on February 18th to 22nd, 2019. The program is started at classroom block with Welcome address by Dr.S.R.Malathi, Associate Professor, EC, SVCE. The course theme and objectives were addressed by Dr.G.A.Sathish kumar Professor, EC.

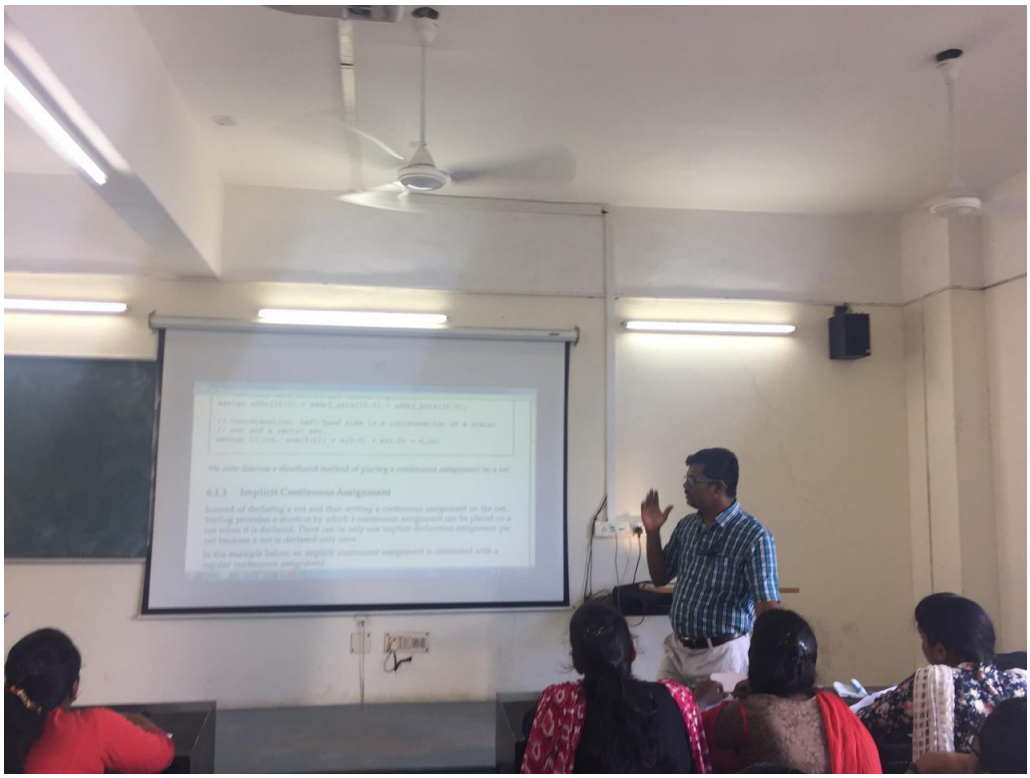
Day 1: The session I was started with a lecture by Dr.G.A.Sathish kumar, Professor, EC with the topics : "Recent Trends in VLSI Technology" in which he discussed starting from the fundamentals (Moore's law) to recent processor trends, VLSI design styles like ASIC and FPGA, latest evolution of VLSI Technology, needs, advantages and applications of VLSI technology. Then he continue his lecture with FinFET's CMOS recent technology by which he explains in detail about the need for FinFET, its development process and its design tradeoffs.

The session 2 was continued by Dr.G.A.Sathish kumar, Professor, EC. Initially, in this session with the title "Overview of Digital Design with Verilog HDL", he discussed the Evolution of Computer-Aided Digital Design, ICs classification, Design flow, emergence, importance and trends in HDL. Consecutively with the topic "Hierarchical Modelling Concepts", he presents about Design methodologies, Verilog- modules, Instances, design block, stimulus block with real time examples in verilog programming language. And under the "Basic Concepts of Verilog HDL", he discussed about lexical conventions, data types, system tasks and compiler directives.

The session 3 starts with a talk about "modules and ports" by Mr.M.Athappan, Asst. Professor, EC, SVCE in which he gives a brief explanation about the components of verilog module- ports, list of ports, port declaration, port connection rules, connecting ports to the external signal and gate level modelling

concepts- Gate types, gate delays, array of instances and examples of Gate level multiplexer, 4-bit ripple carry adder and design examples of S-R Latch.

In day 2, the session 1 was started by Mr.M.Athappan, Asst. Professor, EC with the concept titled “Data Flow Modelling”. This session consists of lectures about continuous assignments, delays, expressions, operators, operands, operator types and examples of 4-to-1 multiplexer, 4-bit full adder and ripple counters in verilog programming language with respective flow of modelling concepts.



The session 2 of day 2 was handled by Dr.S.R.Malathi, Associate Professor, EC, SVCE. She explains the “Behavioural Modelling Concepts” in which she explains the structured procedures, procedural assignments, conditional statements, multiway branching, loops, sequential and parallel blocks. Also, she detailed the examples of 4-to-1 multiplexer, 4-bit counter and Traffic signal Controller through Finite State Machine(FSM) design concept.

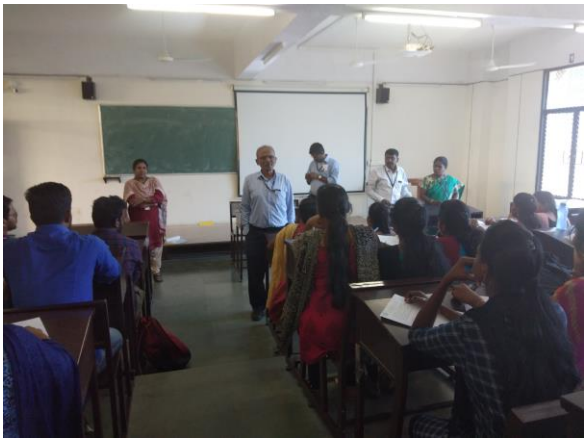
Session 3 was handled by Ms. C.T.Poomagal, Research Scholar, EC, SVCE. She explains the programming flow, how to use the Xilinx ISE software tool to write and execute the codes in verilog HDL and how to simulate the tool to verify the written verilog codes to get the RTL design of some example programs. The participants were started writing verilog program for simple logics like Full Adder, Ripple carry adder(RCA), by their own.

Day 3, session 1 was started with a deep introduction on Tasks and Functions which includes the Function declaration, Function invocation, Recursive functions, Constant functions and signed functions with examples of parity calculator and left/right shifter by Dr.S.R.Malathi, Associate professor, EC. Also, she continued the following topics of Switch level modeling – MOS switches, CMOS switches, Bi-directional switches, Resistive switches with examples of CMOS NOR gate, 2-to-1 MUX, CMOS inverter in session 2.

In session 3, the concepts of Carry look ahead adder, ALU and Booth multiplier were detailed by Ms. C.T.Poomagal, Research Scholar, EC and the hands-on for the above said logic were continued with the usage of case statements, loops, instantiations of other functions, by which the participants could write and executed the codes for Carry look ahead adder, ALU, Booth multiplier in Xilinx 14.7.

In day 4, Dr.S.R.Malathi, Associate professor, EC has given a brief lecture about User defined Primitives (UDP) - UDP basics, combinational UDPs, sequential UDPs, UDP table shorthand symbols in session 1. Then the session 2 with hands-on was handled by Ms. S.M.Mehzabeen, Asst. Professor, EC and Ms. Poomagal, in which the participants were trained to implement the verilog modules into an FPGA board(Spartan 3E) using iMPACT tool of Xilinx software. In session 3, the requirements, constraints and applications of CADANCE software tool and a short introduction on work flow of CADENCE tool were given by Ms.S.M.Mehzabeen, Asst. Professor, EC and Ms.C.T.Poomagal, Research Scholar.

Day 5 was an entire package of hand-on session with CADENCE tool handled by Ms. S.M.Mehzabeen and Ms. C.T.Poomagal at Applied Electronics Laboratory. At the end of session, participants learnt the thorough flow of a digital design using CADENCE tool. Also, they could gain knowledge about the timing analysis, area analysis and generation of .gdc file for fabrication of ASIC models.



The valedictory address by Dr.S.Muthukumar, Professor/HOD, EC and also he distributed the certificates to the participants. Finally, the course concluded with the vote of thanks and the valuable feedbacks from participants.

SRI VENKATESWARA COLLEGE OF ENGINEERING

(Autonomous - Affiliated to Anna University, ISO 9001 : 2015 Certified)

PENNALUR, SRIPERUMBUDUR 602117, TAMILNADU

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Certificate of Participation

This is to certify that Mr./Ms. _____ *has participated in the 5 days value added course on* "HARDWARE MODELING USING VERILOG", *conducted by the Department of Electronics and Communication Engineering, Sri Venkateswara College of Engineering from 18-02-2019 to 22-02-2019*

Course Co-ordinators
Dr.G.A.SATHISHKUMAR
Dr.S.R.MALATHI

Convenor
Dr.S.MUTHUKUMAR

SRI VENKATESWARA COLLEGE OF ENGINEERING

FEEDBACK - INPLANT TRAINING / SHORT TERM COURSE

Name of the Student	V. Nadhiya
Branch/Semester/Section/Roll No.	E.C.E / VIIth B / 160701094
Industry/ Institution Visited	S.V.C.E.
Duration of Training/ Course with date	One week / 18th Feb 2019 - 22nd Feb 2019 5 days.
Plants visited during training	—

Whether the training/Course was useful? In what way? Give reasons.

Yes, the training is very useful. We learn the xilinx process how to Implement.

Any other suggestions

We able to coded in xilinx software, Implement hardware and cadence all are understood. It's very useful for our higher studies and placements

V. Nadhiya
Signature

Report and Copy of Certificate submitted.

HOD

M. Hellan
Faculty Incharge

The person who has attended the course should prepare this in triplicate and submit copies to:
A2, A3 and Dept.

Hardware Modeling using VERILOG (18/2/2019 to 22/2/2019)
A Batch

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B Batch

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10.	71	Keerthi.S.	8754434564	keerthi990207@gmail.com	S. Keerthi
11.	72	Kesavapriya.R.	9952582927	Kesavapriya1999@gmail.com	R. Kesavapriya
12.	62	Jayashri.J	7904742439	jayashrijayaraman13@gmail.com	

M. Sheeran

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