FT/GN/18/06/10.06.15

SRI VENKATESWARA COLLEGE OF ENGINEERING

PROPOSAL FOR PROCUREMENT

Ref: EC/others/2016-17/01

Date:25.07.2016

DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Lab/Section: **ECE -Workshop**

BUDGET HEAD: EQPT/CONS/R&M/AMC/BOOKS/JOURNALS/FUR/BLDG/**OTHERS(workshop)**

Sl. No	Subject Code	A3 Code	Item Description	Qty req.	Tentative cost
1		2.2.6	Two Days Workshop on **"Analog Custom IC Design using Cadence EDA"**	-	7,000/-

Justification by the proposer:
Department is organizing a two days workshop on "Analog Custom IC Design using Cadence EDA" in association with Entuple Technologies Private Ltd., for our P.G Students and faculty from other colleges.

Item: **Budgeted** / Non-budgeted — Date: 25/7/16 — Signature of the Proposer

Comments by the HOD: Recommended — Date: 25/7/16 — Signature of the HOD

Verification by A3 section: Budget 16-16 - Revenue - Balance - Rs. 9.40 Lakhs — Date: 25/7/16 — Signature of the verifying officer

Comments by the Principal: Approved — Date: 25/7/16 — Signature of the Principal

Comments by the Secretary — Date: — Signature of the Secretary

Note : 1. A minimum of 3 quotations are to be obtained, if purchase value exceeds Rs.5,000/-
2. Single quotation to be obtained for any purchase of value between Rs.2000 – 5000/-
3. In case of book purchase, single quotation is accepted.
4. After approval, a copy of this to be retained by the HOD.
5. Quote the Ref. No. in all future communications

SRI VENKATESWARA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SVCE/EC/Workshop/Entuple Technologies/2015-16 21/07/2016

Submitted to the Principal:

Sub: Proposal to organize a Two Days Workshop on Analog Custom IC Design Using Cadence EDA

It has been proposed to organize a Workshop titled "**Analog Custom IC Design Using Cadence EDA**" on 19th & 20th August 2016 for faculty from other colleges and our PG students.

Entuple Technologies Pvt. Ltd., is one of the leading company which offers the Engineering Software Solutions and Industry standard tools, has consented to depute experts to conduct the Workshop at our campus.

We request you to grant the amount 7,000/- towards the programme expenditure and pay us an advance.

It is requested that the above proposal may be approved.

Dr.G.A.Sathish Kumar

Mr.M.Athappan

Mr.S.Saravanan

Coordinators

Dr.S.Muthu Kumar

HoD – EC

Encl:

Budget Estimate

Approved – Brochure need not be printed for fewer number of ext participants

22/7/16.

SRI VENKATESWARA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Two Days Workshop on Analog Custom IC Design Using Cadence EDA

Budget Estimate

Brochure and Course Material Expenses	-	Rs. 3000
Stationary (Delegates Kit)	-	Rs. 1000
Incidental Expenses (Lunch and Refreshments)	-	Rs. 8000
Certificate and Banner Expenses	-	Rs. 2000
Memento and Honorarium	-	Rs. 6000
Traveling expenses & Accommodation	-	Rs. 6000
Miscellaneous Expenses	-	Rs. 1000
Sub Total (Amount received from participant)	-	
20 x 1000	-	Rs. 20,000
Sub Total (Amount requested from our management)	-	Rs. 7,000
Total Expenses	-	**Rs. 27,000/-**

Dr.G.A.Sathish Kumar

Mr.M.Athappan

Mr.S.Saravanan

Coordinators

Dr.S.Muthu Kumar

HoD – EC

DECLARATION

The above information is true to the best of my knowledge. I agree to abide by the rules and regulations governing the course. If selected, I shall attend the course for the entire duration. I also undertake the responsibility to inform the coordinators in case I am unable to attend the course.

Place:

Date: Signature of the Applicant

SPONSORSHIP CERTIFICATE

Mr / Ms / Dr_____

_____ is an employee / student of our institute and is hereby sponsored. He / She will be permitted to attend the course for the entire duration, If selected.

Office Seal

Signature of the Sponsoring authority

Place:

Date:

Application form completed in all aspects is to be sent to:

Dr. G.A.SATHISH KUMAR
Professor
Co-ordinator

Dept of Electronics and Communication Engg,
SRI VENKATESWARA COLLEGE OF ENGINEERING
Post Bag No.1, Pennalur Village
Chennai - Bengaluru High Road
Sriperumbudur Tk. - 602 117
Kancheepuram District
TAMIL NADU.

RESOURCE PERSONS

Sessions will be handled by experts from ENTUPLE Technologies, Bengaluru.

ELIGIBILITY

Personnel from AICTE approved Engineering Colleges (PG Students), Industries and Research Scholars.

REGISTRATION

Registration fee: **Rs.1000**

HOW TO APPLY

The applicants should send their applications in the specified format along with a DD drawn in favor of **"The Principal, Sri Venkateswara College of Engineering"**, payable at Indian Bank, Sriperumbudur should reach on or before **13.08.2016.** If selected, they should confirm their participation as per schedule below.

SCHEDULED DATES

Last Date for Receipt of Applications : 13.08.2016

Intimation of Selection by e-mail : 16.08.2016

TRANSPORT

The participants can avail the SVCE bus facility to attend this workshop, For transportation details, please refer our college website.

SRI VENKATESWARA COLLEGE OF ENGINEERING

(Autonomous - Affiliated to Anna University)

(An ISO 9001:2008 Certified College)

PRESENTS

"TWO DAYS WORKSHOP ON ANALOG CUSTOM IC DESIGN USING CADENCE EDA"

19th and 20th August , 2016

CONVENOR
Dr.S.MUTHUKUMAR, HOD/EC

CO-ORDINATORS

Dr.G.A.SATHISH KUMAR, Professor

Mr.M.ATHAPPAN, Assistant Professor

Mr.S.SARAVANAN, Assistant Professor

Organized by

Dept. of Electronics & Communication Engg.,
SRI VENKATESWARA COLLEGE OF ENGINEERING

Mobile: 9445265296,9445205156,9884806830

Tel: 044-27152000, Ext: 201, 203.

E-mail: sathish@svce.ac.in
athappan@svce.ac.in
saravanans@svce.ac.in
Website: www.svce.ac.in

THE PROGRAMME CONTENTS OF THE WORKSHOP ARE AS FOLLOWS:

Introduction to VLSI, PDK Device Characterization for Analog Model Parameters like MOS characterization-Illustration and hands-on, I-V characteristics, Effective switching resistances, Pin capacitances, Development of circuit topology inverter from fundamentals.

CMOS inverter and its applications, Concept of balanced, symmetric and fastest inverter. Hands – on lab: Design and Simulation of a balanced CMOS inverter, Analysis of the quality metrics of designed inverter-Propagation delay, Power consumption, Noise Margin.

Custom IC design flow of designed balanced inverter, Hands – on Lab: Layout, DRC, LVS, Parasitic extraction, Post Layout Simulation with parasitic back annotation, GDSII of the layout.

Review of the generic amplifier performance parameters – Gain, Power Dissipation, Frequency Response (UGB, BW), Synthesis of CS Amplifier Circuit Topologies – Resistive load, Diode connected, Current source load, Interpreting the Design Specifications, Design and simulation of CS Amplifier with current source load: DC and small signal AC performance.

Analog Layout Design Concepts – Importance of Device Matching in Layouts, Layout, DRC, LVS, Parasitic extraction, Post Layout Simulation with parasitic back annotation, GDSII of the layout.

ABOUT THE INSTITUTION

Sri Venkateswara College of Engineering (SVCE), one of the Premier Technical Institutions in Tamilnadu, was established in 1985, approved by AICTE New Delhi and affliated to Anna University, chennai has completed 30 years of dedicated and excellent service in the field of technical education. The College is situated on the Chennai – Bangalore National Highway (NH4) about 37 km south-west of Chennai. The college offers 10 UG programmes and 10 PG programmes. The National Board of Accreditation has accredited many of the eligible programmes, and SVCE is an ISO 9001:2008 certified institution.

ABOUT THE DEPARTMENT

The Electronics and Communication Engineering department occupies a prominent place in the chronicles of its academic history. The specialization of the faculty includes Telecommunication engineering, Computer Networks, Control Systems, VLSI, Digital Signal Processing, Microwave Systems, Applied Electronics, Microprocessor and Micro Controllers etc. The department has excellent laboratory facilities in the areas like Networking, Microprocessors & Microcontrollers, Electronic Devices, Communication, RF, Microwave, VLSI, Digital Signal Processing, Applied Electronics, with latest software. The department offers four year UG programme in ECE and two year PG programmes in Communication Systems and Applied Electronics. The department is a approved research center by Anna University. Around 40 Research scholars are pursuing their full time and part time Ph.D in the research center.

SRI VENKATESWARA COLLEGE OF ENGINEERING
(Autonomous - Affiliated to Anna University)

Post Bag No.1, Pennalur Village
Chennai - Bengaluru High Road
Sriperumbudur Tk. - 602 117
Kancheepuram District, TAMIL NADU.
PRESENTS

"TWO DAYS WORKSHOP ON ANALOG CUSTOM IC DESIGN USING CADENCE EDA"

19th and 20th August, 2016

APPLICATION FORM

Name:

Department:

Educational Qualification:

Age:

Organization:

Designation:

Address for Communication:

E-mail ID:

Mobile Number:

Signature of the Sponsoring Authority

Signature of the Applicant

SRI VENKATESWARA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PENNALUR, SRIPERUMBUDUR TALUK, 602117

TWO DAYS WORKSHOP ON ANALOG CUSTOM IC DESIGN USING CADENCE EDA

Agenda

Day 1(19/08/2016- Friday):

8:30 – 9:00 am	: Registration.
9:00 am	: Prayer song.
9:10 – 9:30 am	: Welcome address.
9:30 – 10:30 am	: PDK Device Characterization for Analog Model Parameters and Development of circuit topology inverter from fundamentals by Mr. Binu Alias.
10:30 – 11:00 am	: Tea break.
11:00 – 12:30 pm	: Custom IC design flow of designed balanced inverter.
12:30 – 1:30 pm	: Lunch.
1:30 – 3:15 pm	: Hands - on training on Design and Simulation of a balanced CMOS inverter.

Day 2(20/08/2016- Saturday):

9:00 – 10:15 am	: Review of the generic amplifier performance parameters by Mr. Binu Alias.
10:15 – 10:45 am	: Tea break.
10:45 – 12:30 pm	: Design and simulation of CS Amplifier with current source load.
12:30 – 1:30 pm	: Lunch.
1:30 – 2:30 pm	: Hands- on training on Analog Layout Design Concepts – Importance of Device Matching in Layouts.
2:30 – 3:15 pm	: Valedictory function.

SRI VENKATESWARA COLLEGE OF ENGINEERING
(Autonomous - Affiliated to Anna University)

Post Bag No.1, Pennalur Village
Chennai - Bengaluru High Road
Sriperumbudur Tk. - 602 117
Kancheepuram District, TAMIL NADU.
PRESENTS

"TWO DAYS WORKSHOP ON ANALOG CUSTOM IC DESIGN USING CADENCE EDA"

19th and 20th August, 2016

APPLICATION FORM

Name:	Dr. S.R. Malathi
Department:	ECE
Educational Qualification:	M.E - Ph.D
Age:	46
Organization:	SVCE
Designation:	Assoc. Professor
Address for Communication:	Dept. Of ECE, SVCE
E-mail ID:	malathiraj@svce.ac.in
Mobile Number:	9962534922

Signature of the Sponsoring Authority

Signature of the Applicant

FT/GN/29A/04/30.06.2016

SRI VENKATESWARA COLLEGE OF ENGINEERING

FEEDBACK – CONFERENCE / SEMINAR / WORKSHOP / FDP

Name of the Faculty/Staff	S.R. MALATHI
Designation & Department	Associate Prof. / ECE
Industry / Institution Visited	—
Duration of Training / Course with date	2 Days Workshop / 19-8-2016 & 20-8-2016
Details of the Training / Course	Two Days Workshop on Analog Custom IC Design using Cadence EDA at SVCE
Plants visited during training	—

Whether the training/Course was useful? In what way? Give reasons.

Yes the training was very useful. This tool, which is widely used in industry for system design, can now be used for implementing VLSI Projects.

Any other suggestions

→ The training could have been conducted on a day when there is no teaching work or any other duties. Because I lost continuity since due to invigilation duties

Signature
Malathi

Effectiveness review by HoD

Based on the interactions with the faculty, this workshop on IC design was very useful and informative.

Signature of HoD

The person who has attended the course should prepare this in triplicate and submit copies to: **A1, A3 and Dept**.

SRI VENKATESWARA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TWO DAYS WORKSHOP ON ANALOG CUSTOM IC DESIGN USING CADENCE EDA

REGISTRATION DETAILS

S.NO	NAME	DESIGNATION	INSTITUTION	DD/CASH	SIGNATURE
1.	ARAVINDHAN K	STUDENT	SVCE	PAID	K. Ar
2.	DEEPA T	STUDENT	SVCE	PAID	T. Deepa.
3.	DEEPIKA G	STUDENT	SVCE	PAID	G
4.	MAGESHWARI N	STUDENT	SVCE	PAID	N. Magesh
5.	NADAR JAMES FRANCIS JOSEPH ROY	STUDENT	SVCE	PAID	
6.	PAVITHRA G	STUDENT	SVCE	PAID	
7.	SWETHA K	STUDENT	SVCE	PAID	K. Swetha
8.	YUVARAJ E	STUDENT	SVCE	PAID	
9.	JENCY RUBIA	SCHOLAR	SVCE	PAID	
10.	N.KUMARAN	FACULTY	SVCE	PAID	
11.	M.ANUSHYA	FACULTY	SVCE	PAID	
12.	M.VIDYA	FACULTY	SVCE	PAID	
13.	R.KOUSALYA	FACULTY	SVCE	PAID	
14.	B.SARALA	FACULTY	SVCE	PAID	
15.	POOMAGAL. C. T.	Research Scholar	SVCE		
16.	M.K.VARADARAJAN	FACULTY	SVCE	Paid.	
17.	A. Bharathi priya	Faculty	SVCE	Paid	
18.	S. Kalyani	faculty	SVCE	Paid	
19.	S. R MALATHI	faculty	SVCE	Paid	
20.	L. ANJU	FACULTY	SVCE	paid	
21.	G. Logarathar	Faculty	SVCE	paid	
22.	P. ARUL	Faculty	SVCE	Paid	
23.	S. RADHIKA	Faculty	SVCE	Paid	
24.	S. SENTHIL RAJAN	FACULTY	SVCE	Paid	
25.	P. Ponsudha	Faculty	Velammal Engg College	Paid	
26.	S. REETHI	Faculty	SVCE	Paid	S. Reethi
27.	P Madhumitha	Faculty	SVCE	Paid	
28.					
29.					
30.					

Sri Venkateswara College of Engineering

Sriperumbudur-602117

Certificate of Participation

This is to certify that Mr/~~Ms~~ YUVARAJ . E

of SRI VENKATESWARA COLLEGE OF ENGINEERING has attended

"TWO DAYS WORKSHOP ON ANALOG CUSTOM IC DESIGN USING CADENCE EDA"

held on 19TH & 20TH August, 2016

Co-ordinator

Convenor

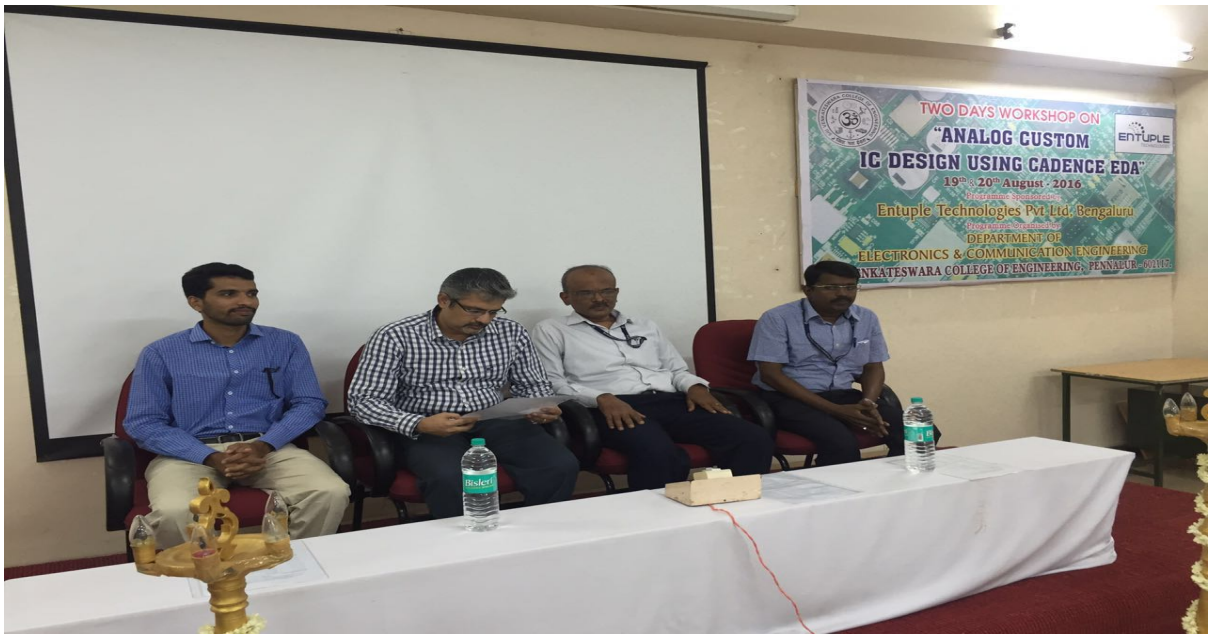
ORGANISED BY

Department of Electronics and Communication Engineering

A Report on "Analog Custom IC Design using Cadence EDA" Workshop Organised during 19th and 20th August 2016

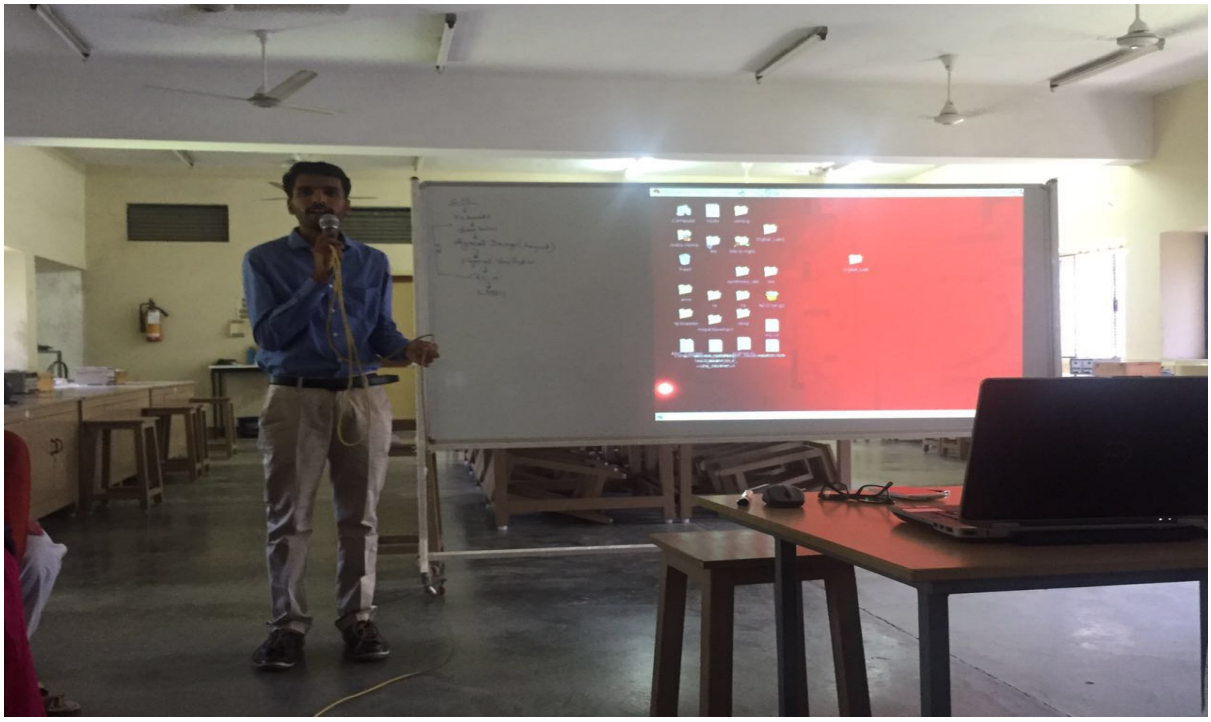
The Two Day 'Workshop on Analog Custom IC Design using Cadence EDA' was held on August 19th and 20th ,2016 conducted by Electronics and Communication Engineering Department, SVCE in association with Entuple Technologies Private Limited Bengaluru. The workshop started with the prayer song by Ms.KeerthiPriya. The Workshop theme was inaugurated with lighting of Kuthu-Vilakku by the Principal.

The Special Address was given by Dr.S.Ganesh Vaidyanathan, Principal and the Welcome address was given by Dr.S.Muthukumar, Head of the Department (ECE). The introduction to Entuple Technologies Private Limited was shared by Dr.G.A.Sathish Kumar, Professor, ECE.

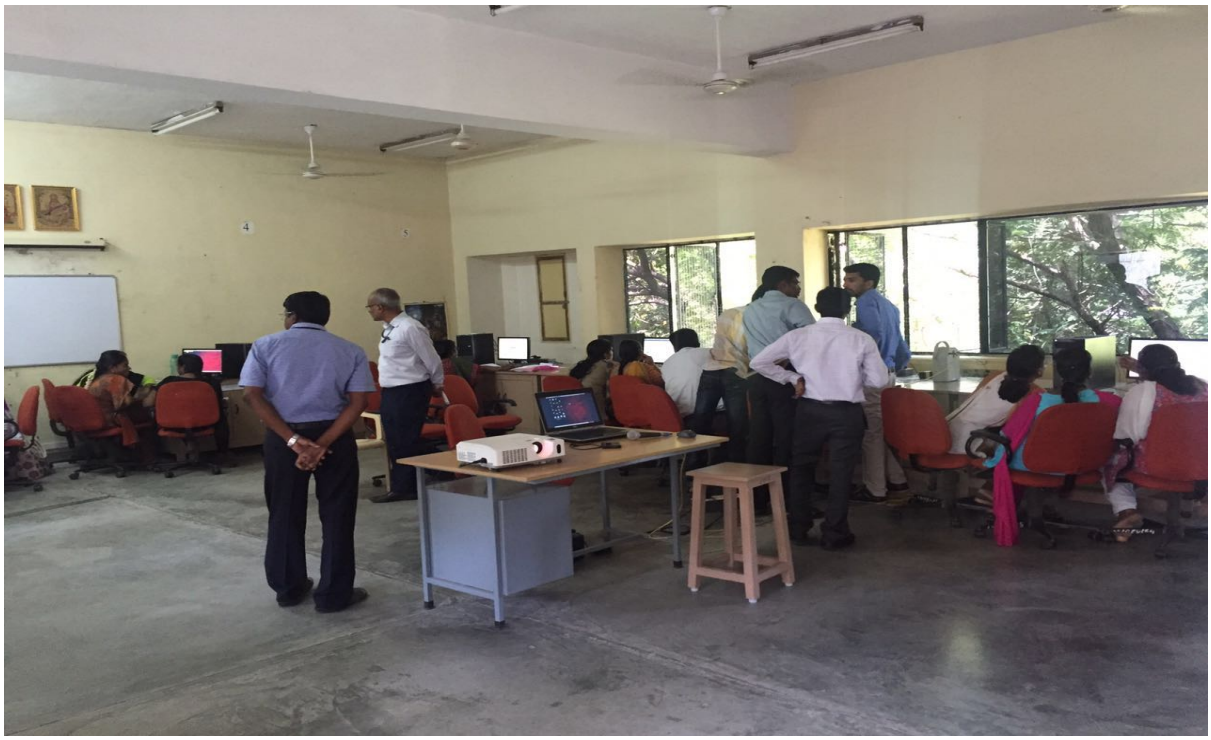


Day1:

The Key Note address on ‘PDK Device Characterization for Analog Model Parameters’ is given by Mr.Binu Alias. The speaker also discussed about the architecture development of circuit topology inverter from fundamentals.

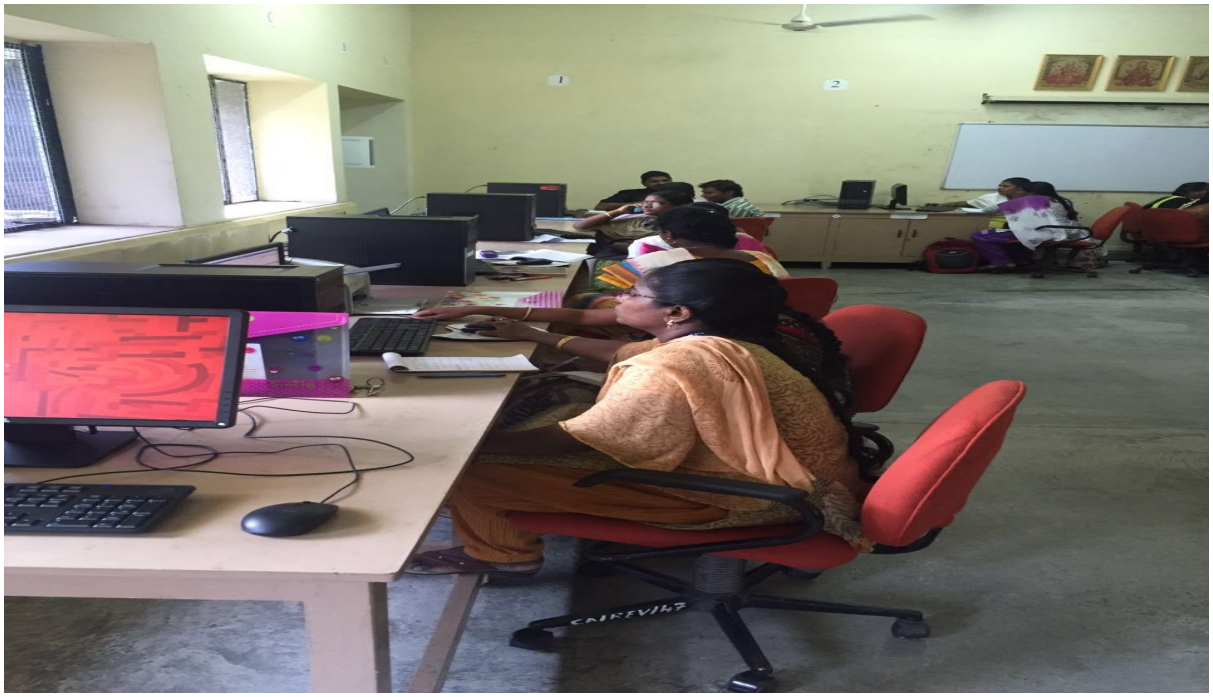


In the afternoon session, hands-on implementation of the Design and Simulation of a balanced CMOS inverter was taught. Custom IC design flow of designed balanced inverter was also taught.

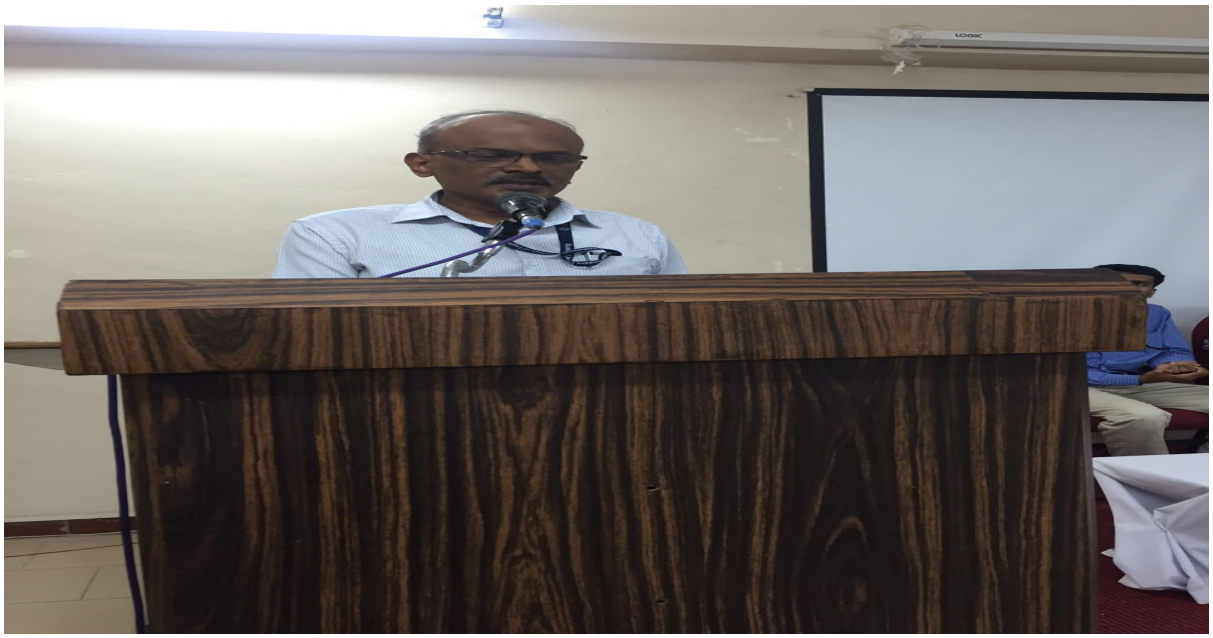


Day2:

The Key Note address was given by Mr.Binu Alias. The speaker in first session spoken about the Review of the generic amplifier performance parameters such as Gain, Power Dissipation and Frequency Response. The speaker also briefed about Design and simulation of CS Amplifier with current source load.



The second session involved hands-on training on the Analog Layout Design Concepts such as Layout, DRC, LVS, Parasitic extraction, Post Layout Simulation with parasitic back annotation and GDSII of the layout.



The valedictory address was given by Dr.S.Muthukumar, Head of the Department (ECE), the momento was given to the Speaker Mr.Binu Alias, Entuple Technologies Private Limited. The certificates were also distributed by HOD/ECE to the participants. The vote of thanks was

given by Mr. Joshua Roshan Samuel Michael, Student (ECE). Finally the day was wrapped up with the National Anthem.