SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY 

| **Department of Electronics and Communication Engineering** | LP: **EC22042** |
|---|---|
| B.E/~~B.Tech~~/~~M.E~~/~~M.Tech~~ : **ECE** Regulation: **2022(Autonomous)** | Rev. No: **00** |
| PG Specialization : **Not Applicable** | **Date:05-07-2024** |
| Sub. Code / Sub. Name : **EC22042 - ASIC AND FPGA DESIGN** | |
| Unit : **I** | |

**Unit Syllabus: OVERVIEW OF ASIC AND PLD (9)**

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

**Objective**: To get familiar with the different types of programming technologies and logic devices

| Session No* | Topics to be covered | Ref | Teaching Aids |
|---|---|---|---|
| 1. | Introduction, Types of ASICs – Full Custom ASIC, Standard Cell Based ASIC. | 1 | ICT |
| 2. | Types of ASICs – Gate Array Based ASIC, Channel Gate Array, Channel less Gate array, Structured Gate Array | 1 | ICT |
| 3. | Programmable Logic Devices, Field Programmable Gate Arrays; Design flow, CAD tools used in ASIC Design, Comparison between ASIC Technologies | 1,2 | ICT |
| 4. | Programming Technologies: Anti fuse, Metal-Metal Anti fuse; Static RAM. | 1,2,9 | ICT |
| 5. | EPROM and EEPROM Technology, Practical Issues, Specification, PREP Benchmark. | 1,2,9 | ICT |
| 6. | Programmable Logic Devices: ROMs, EPROMs, Programmable Logic Array (PLA). | 1,2,5 | ICT |
| 7. | Programmable Array Logic (PAL). | 1,5 | ICT |
| 8. | Gate Arrays – CPLDs, FPGAs | 1,2, 6,9 | ICT |
| 9. | Gate Arrays – CPLDs, FPGAs | 1,2, 6,9 | ICT |
| | **Content beyond syllabus covered (if any): NIL** | | |

* Session duration: 50 minutes

Sub. Code / Sub. Name: **EC22042 - ASIC AND FPGA DESIGN**

Unit: **II**

**Unit Syllabus: ASIC PHYSICAL DESIGN (9)**

System partition - partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing global routing - detailed routing - special routing – circuit extraction - DRC

**Objective**: To acquire knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC

| Session No * | Topics to be covered | Ref | Teaching Aids |
|---|---|---|---|
| 10. | System partitioning: Goals and objectives, FPGA Partitioning | 1, 9 | ICT |
| 11. | Partitioning methods: Constructive and Iterative partitioning algorithms, | 1, 9 | ICT |
| 12. | Partitioning methods: The Kernighan-Lin Algorithm, The Ratio Cut Algorithm, The Look-ahead Algorithm, Simulated Annealing algorithm | 1, 9 | ICT |
| 13. | Floor planning: Goals and objectives, measurement of delay, Channel Definition, I/O and Power Planning, Clock planning | 1, 9, 13, 14 | ICT |
| 14. | Placement: Terms, Definitions, Goals and Objectives, Measurement of Goals and Objectives, Placement Algorithms – Eigenvalue placement | 1, 9 | ICT |
| 15. | Iterative placement improvement, Placement using Simulated Annealing, Time Driven placement method | 1, 9 | ICT |
| 16. | Routing: Goals and Objectives, Measurement of Interconnect delay, Global Routing – between blocks – inside flexible blocks – timing driven methods – back annotation method | 1, 9 | ICT |
| 17. | Detailed Routing – Goals and objectives – Measurement of Channel Density – Algorithms: Left Edge Algorithm – Constraints and Routing graph | 1, 9 | ICT |
| 18. | Detailed Routing – Area Routing Algorithm – Multilevel Routing – Timing Driven Detailed Routing, Special routing, Circuit extraction, DRC. | 1, 9 | ICT |
| | **CAT - 1** | | |
| **Content beyond syllabus covered (if any):** NIL | | | |

* Session duration: 50 mins

Sub. Code / Sub. Name: **EC22042 - ASIC AND FPGA DESIGN**

Unit: **III**

**Unit Syllabus: LOGIC SYNTHESIS, SIMULATION AND TESTING (9)**

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation

**Objective**: To analyze the synthesis, simulation and testing of systems

| Session No * | Topics to be covered | Ref | Teaching Aids |
|---|---|---|---|
| 19. | Design systems - Logic Synthesis | 1 | ICT |
| 20. | Half gate ASIC, Schematic entry | 1 | ICT |
| 21. | Low level design language, PLA tools | 1, 5 | ICT |
| 22. | EDIF- CFI design representation | 1 | ICT |
| 23. | Verilog and logic synthesis | 1 | ICT |
| 24. | VHDL and logic synthesis | 1 | ICT |
| 25. | Types of simulation, Boundary scan test | 1 | ICT |
| 26. | Fault simulation, Automatic test pattern generation. | 1 | ICT |
| 27. | Formal Verification: An Example, Understanding Formal verification – Adding Assertion – Completing a proof | 1 | ICT |
| **Content beyond syllabus covered (if any):** NIL | | | |

* Session duration: 50 mins

Sub. Code / Sub. Name: **EC22042 - ASIC AND FPGA DESIGN**

Unit: **IV**

**Unit Syllabus: FPGA Fabrics 9**

Introduction, FPGA Architectures; SRAM-Based FPGAs; Permanently Programmed FPGAs; Chip I/O; Circuit Design of FPGA Fabrics; Architecture of FPGA Fabrics

**Objective:** To learn the architecture of different types of FPGA

| Session No * | Topics to be covered | Ref | Teaching Aids |
|---|---|---|---|
| 28. | Introduction - FPGA Fabrics | 1,2,6,9, 10, 11 | ICT |
| 29. | SRAM-Based FPGAs - I | 1,2,6,9 | ICT |
| 30. | SRAM-Based FPGAs - II | 1,2,6,9 | ICT |
| 31. | SRAM-Based FPGAs – III | 1,2,6,9 | ICT |
| 32. | Permanently Programmed FPGAs | 1,2,6 | ICT |
| 33. | Chip I/O | 1,2,6 | ICT |
| 34. | Circuit Design of FPGA Fabrics | 1, 6 | ICT |
| 35. | Circuit Design of FPGA Fabrics - Tutorial | 1,2,9,11 | ICT |
| 36. | Architecture of FPGA Fabrics | 6,9,11 | ICT |
| **Content beyond syllabus covered (if any):** NIL | | | |

* Session duration: 50 mins

Sub. Code / Sub. Name: **EC22042 - ASIC AND FPGA DESIGN**

Unit: **V**

**Unit Syllabus: SOC DESIGN 9**

Design Methodologies – Processes and Flows - Embedded software development for SOC – Techniques for SOC Testing – Configurable SOC – Hardware / Software co-design Case studies: Digital camera, Bluetooth radio / modem, SDRAM and USB

**Objective**: To understand the design issues of SOC

| Session No * | Topics to be covered | Ref | Teaching Aids |
|---|---|---|---|
| 37. | Introduction to SOC, Design Methodologies | 8,10 | ICT |
| 38. | Processes and Flows | 8,10 | ICT |
| 39. | Embedded software development for SOC | 8,10 | ICT |
| 40. | Techniques for SOC Testing | 8,10 | ICT |
| 41. | Configurable SOC | 8,10 | ICT |
| 42. | Hardware / Software co-design | 8,10 | ICT |
| 43. | Digital camera | 8,10 | ICT |
| 44. | Bluetooth radio | 8,10 | ICT |
| 45. | Modem, SDRAM and USB | 8,10 | ICT |
| | CAT - 2 | | |
| **Content beyond syllabus covered (if any):** NIL | | | |

* Session duration: 50 mins

Sub Code / Sub Name: **EC22042 - ASIC AND FPGA DESIGN**

**TEXTBOOKS:**

1. M.J.S.Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc.,1997
2. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
3. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, PrenticeHall, 1994.

**REFERENCES:**

4. S.Trimberger, Field Programmable Gate Array Technology, Edr, Kluwer Academic Publications, 1994.
5. John V.Oldfield, Richard C Dore, Field Programmable Gate Arrays, Wiley Publications 1995.
6. Parag.K.Lala, Digital System Design using Programmable Logic Devices , BSP, 2003.
7. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
8. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 995.
9. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
10. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
11. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

| | Prepared by | Approved by |
|---|---|---|
| **Signature** | Malathi | |
| **Name** | Dr. S. R. Malathi | Dr. G.A. Sathish Kumar |
| **Designation** | Professor | Professor and Head |
| **Date** | 05.07.2024 | 09.07.2024 |

**Remarks *:** Same course delivery plan is followed in the academic year 2024-25 EVEN Semester also. Malathi 20/1/2025

**Remarks *:**

**Remarks *:**