Q. Code: 996829

Reg. No. | | | | | | | | | | | | | |

B.E./ B.TECH. DEGREE EXAMINATIONS, MAY 2024

Second Semester

IT22201– COMPUTER ORGANIZATION AND ARCHITECTURE

(Information Technology)

(Regulation2022)

TIME:3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Build the basic structure of computer, operations and instructions.	**4**
CO 2	Design arithmetic and logic unit.	**5**
CO 3	Design and analyze pipelined control units.	**5**
CO 4	Evaluate performance of memory systems.	**5**
CO 5	Construct the parallel processing architectures.	**5**

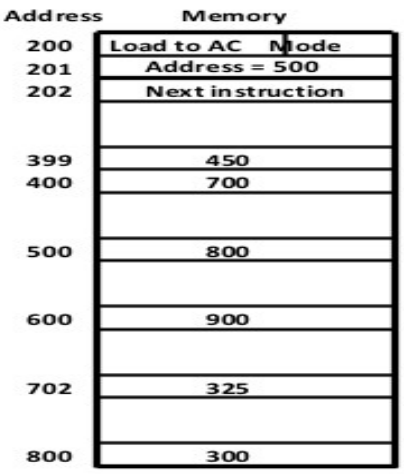
PART- A(20x2=40Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Estimate the effective address to fetch the operand from the memory location 1350 pointed by memory location 300.	**1**	**2**
2.	Sketch the basic computer instruction code format.	**1**	**3**
3.	Identify the size of below registers. a. PC b. DR c. INPR d. OUTR	**1**	**2**
4.	Examine the value of FGI when an 8-bit alphanumeric code is shifted into INPR.	**1**	**3**
5.	Construct the flowchart for Booth's multiplication algorithm.	**2**	**3**
6.	Compare the observations on MULTIPLICATION algorithm V1 and V2	**2**	**4**
7.	Write a code to check stack overflow and underflow condition when the stack pointer is at the location 3000.	**2**	**3**
8.	Differentiate polish notation from reverse polish notation.	**2**	**4**
9.	Identify the two state elements needed to store and access an instruction.	**3**	**2**
10.	Differentiate exception from interrupt.	**3**	**4**
11.	Justify the following statement. Forwarding represents a viable solution for mitigating data hazards.	**3**	**5**
12.	Illustrate the effect of prediction success and failure in Branch prediction.	**3**	**3**
13.	Distinguish Temporal locality from Spatial locality.	**4**	**4**
14.	Examine how the data is transferred between two adjacent levels in memory hierarchy.	**4**	**3**
15.	Compute the block to map between address and cache locations for a direct mapped cache (assume 8 blocks in the cache).	**4**	**3**

16.	Distinguish between Memory mapped and Isolated I/O.	**4**	**4**
17.	Summarize the challenges in the parallel processing programs.	**5**	**2**
18.	Analyze how four threads use the issue slots of a superscalar processor in different approaches.	**5**	**4**
19.	Identify and categorize the fundamental assumptions made in the design and operation of GPUs for parallel computing.	**5**	**2**
20.	Construct a conditional code for different processors to execute in MIMD.	**5**	**3**

PART- B (5x 10=50Marks)

		Marks	CO	RBT LEVEL
21.(a)	Sketch the complete process logic to synchronize the timing rate difference between the input/output device and the computer.	**(10)**	**1**	**3**
	(OR)			
(b)	Develop a logic using Gate structures for controlling the LD, INR, and CLR of Accumulator register.	**(10)**	**1**	**3**
22.(a)	Solve –0.75ten and represent in IEEE 754 single precision.	**(10)**	**2**	**3**
	(OR)			
(b)		**(10)**	**2**	**3**

PC=202, R1=400, XR=100, AC

Calculate Direct address, Immediate operand, Indirect address, Relative address, Indexed address, register, Register indirect, Auto increment and auto decrement addressing modes using the data and address in the memory.

23.(a)	Choose the appropriate control line to build data path and control for	**(10)**	**3**	**5**

register, branch, load and store instructions.

(OR)

(b)	Consider a loop branch that branches nine times in a row, then is not taken once. What is the prediction accuracy for this branch, assuming the prediction bit for this branch remains in the prediction buffer?	**(10)**	**3**	**5**
24.(a)	Illustrate how cache miss and writes are handled by the processor.	**(10)**	**4**	**2**

(OR)

(b)	Demonstrate on a technique used for high-speed I/O device to transfer data directly to or from the memory, without continuous involvement by the processor.	**(10)**	**4**	**2**
25.(a)	Analyze the implications of selecting a specific Flynn's classification category on the design and implementation of the computer system in detail.	**(10)**	**5**	**4**

(OR)

(b)	Evaluate the advantages and limitations of utilizing a shared memory architecture in SMP systems compared to other multiprocessing architecture.	**(10)**	**5**	**4**

PART- C (1x 10=10Marks)

(Q.No.26 is compulsory)

		Marks	CO	RBT LEVEL
26	Critically analyze the potential sources of error or inefficiency in the non restoring division algorithm and propose strategies for mitigating these issues by solving the dividend 4 and the divisor 2.	**(10)**	**2**	**4**

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