Q. Code:569924

Reg. No. | | | | | | | | | | | | | |

B.E./ B. TECH.DEGREE EXAMINATIONS, MAY 2024

Third Semester

IT18302 –COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation2018/2018A)

TIME:3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Build the basic structure of computer, operations and instructions	**4**
CO 2	Design arithmetic and logic unit.	**6**
CO 3	Design and analyze pipelined control units	**6**
CO 4	Evaluate performance of memory systems.	**5**
CO 5	Construct the parallel processing architectures.	**6**

PART- A(10x2=20Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	List out the phases in the instruction cycle.	**1**	**1**
2.	How would you categorize the process by which the CPU identifies the origin of an interrupt request?	**1**	**1**
3.	Sketch the IEEE 754 Floating-point Standard for two word number.	**2**	**3**
4.	Identify the micro operation for the below control word 010 011 001 00101	**2**	**3**
5.	Analyze the load and store instruction.	**3**	**4**
6.	Compare and contrast the solutions for data hazards.	**3**	**4**
7.	Summarize the size of memory at each level.	**4**	**2**
8.	Examine the I/O interface for an I/O device.	**4**	**4**
9.	Distinguish Scalar instruction from vector instruction.	**5**	**4**
10.	Analyze how the implementation of the following two optimizations alleviates computational bottlenecks in most kernel operations?	**5**	**4**

PART- B (5x 14=70Marks)

		Marks	CO	RBT LEVEL
11. (a)	Examine on the two micro operations DR←AC and AC←DR (Exchange) executed at the same time in the 16 bit common bus architecture in detail.	**(14)**	**1**	**3**

(OR)

(b)	Employ the basic logic gates and design accumulator logic.	**(14)**	**1**	**3**
12. (a)	Apply the method for solving multiplication of 8 by 2, utilizing the last version of the multiplication algorithm.	**(14)**	**2**	**3**

(OR)

(b)	Illustrate the procedure for computing the product of 4 multiplied by 2, employing the initial version of the multiplication algorithm.	**(14)**	**2**	**3**
13. (a)	Assess the efficiency of the designed data path and control lines for load and store instructions compared to alternative designs.	**(14)**	**3**	**5**

(OR)

(b)	Estimate and choose appropriate solutions and alternatives for data, structural and control hazards in pipeline.	**(14)**	**3**	**5**
14. (a)	Compare and contrast different cache mapping techniques.	**(14)**	**4**	**4**

(OR)

(b)	Analyze how different I/O techniques impact the system resources and overall system efficiency in detail.	**(14)**	**4**	**4**
15. (a)	Illustrate how four threads use the issue slots of a superscalar processor in different approaches?	**(14)**	**5**	**3**

(OR)

(b)	Identify specific scenarios where the assumptions and limitations of GPUs become critical factors in system design and performance optimization.	**(14)**	**5**	**3**

PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Devise an efficient algorithm to perform arithmetic operations over two floating point numbers.	**(10)**	**2**	**4**

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