Q. Code:874663

Reg. No. | | | | | | | | | | | | | |

B.E./ B. TECH.DEGREE EXAMINATIONS, MAY 2024

Eighth Semester

EE18702 – VLSI AND EMBEDDED SYSTEMS

(Electrical and Electronics Engineering)

(Regulation 2018)

TIME:3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Learn about the VLSI design process and its properties.	**4**
CO 2	Acquire knowledge to design combinational circuits using MOS.	**4**
CO 3	Acquire knowledge about embedded system and processors and their applications.	**4**
CO 4	Learn about the networking protocols and its applications.	**5**
CO 5	Understand the concepts of RTOS in embedded system	**5**

PART- A(10x2=20Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Distinguish the functionalities of depletion mode and enhancement mode for NMOS transistors.	**1**	**3**
2.	Using appropriate color coding, sketch a stick diagram for CMOS 2-input NAND gate	**1**	**3**
3.	Sketch the dynamic CMOS logic using 2-NOR gates.	**2**	**3**
4.	What are the advantages of transmission gate in terms of logic?	**2**	**3**
5.	Briefly enumerate the classifications of embedded system in terms of complexity?	**3**	**2**
6.	Compare timer, counter and watch dog timer.	**3**	**3**
7.	What is the role of SBUF in serial communication?	**4**	**2**
8.	Distinguish between half duplex and full duplex with suitable examples.	**4**	**3**
9.	How are threads different from tasks?	**5**	**3**
10.	Compare binary and mutex semaphore	**5**	**2**

PART- B (5x 14=70Marks)

		Marks	CO	RBT LEVEL
11. (a)	Discuss in detail, the various steps involved in VLSI design flow.	**(14)**	**1**	**3**
	(OR)			
(b)	Discuss the different regions in CMOS inverter-current characteristics and derive the expression related to region.	**(14)**	**1**	**3**
12. (a)	Design a CMOS logic for implement the following expression.	**(14)**	**2**	**4**

X= $\overline{A.(BC)' + D.E}$
$Y = \overline{(A + BC) + D}$

(OR)

(b)	Analyze the dynamic and clocked CMOS logic with a simple example.	**(14)**	**2**	**4**
13. (a)	Sketch the structural units in embedded processor and demonstrate their functions in detail.	**(14)**	**3**	**3**

(OR)

(b)	Illustrate the virtual memory and cache memory management schemes in embedded system with neat diagrams.	**(14)**	**3**	**3**
14. (a)	Identify the standard network protocol of embedded systems in automobile embedded system. Depict the interface with a neat block diagram. Explain the frame bit format.	**(14)**	**4**	**4**

(OR)

(b)	Sketch the SPI bus serial communication protocol and describe the same.	**(14)**	**4**	**4**
15. (a)	Explain in detail about the thread, thread stack, task and task control block.	**(14)**	**5**	**4**

(OR)

(b)	Discuss in detail about the inter process communication concept in Mailbox.	**(14)**	**5**	**4**

PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Design an 8:1 MUX using transmission gates. Write its logical expression and also draw its schematic diagram.	**(10)**	**2**	**4**

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