Q. Code:858529

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2024

Fourth Semester

EE18402 – DIGITAL LOGIC CIRCUITS

(ELECTRICAL AND ELECTRONICS ENGINEERING)

(Regulation 2018 /2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Understand various aspects of Boolean algebra.	**2**
CO 2	Design and evaluation of combinational logic circuits.	**5**
CO 3	Design and evaluation of sequential logic circuits.	**5**
CO 4	Design and analysis of asynchronous sequential logic circuits through VHDL.	**5**
CO 5	Comprehend the operation and characteristics of memory devices and digital logic families.	**3**

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Convert the $(137255)_8$ to its equivalent number in base 16.	**1**	**2**
2.	State De-Morgan's laws of Boolean algebra.	**1**	**2**
3.	Draw the logic diagram of full adder circuit.	**2**	**3**
4.	Validate the importance of parity generator and parity checker logic circuits.	**2**	**4**
5.	Summarize the State Assignment Rules.	**3**	**2**
6.	Compare Mealy and Moore model.	**3**	**2**
7.	Differentiate synchronous and asynchronous sequential circuits.	**4**	**2**
8.	Present a VHDL coding for EX-OR logic gate.	**4**	**3**
9.	Define fan-in and fan-out.	**5**	**2**
10.	Compare PAL with PROM.	**5**	**2**

PART- B (5 x 14 = 70 Marks)

			Marks	CO	RBT LEVEL
11. (a)		Simplify the following using K map and realize the reduced function using NAND gates only. $\sum$**m(1,2,4,5,7,9,12,13)+ .$\sum$d(3,8)**	**(14)**	**1**	**2**
		(OR)			
(b)	**(i)**	Obtain the canonical SOP & POS of the following expression **Y=A+AB+BC**	**(8)**	**1**	**2**
	(ii)	Obtain the truth table and minterms of the function. **F=xy+xy'+y'z.**	**(6)**	**1**	**2**

12. (a)	Design and implement Binary to gray code converter.	**(14)**	**2**	**4**
	(OR)			
(b)	**(i)** Realize full adder logic with **3 : 8** decoder circuit.	**(7)**	**2**	**4**
	(ii) Design and implement **8X1** multiplexer using basic gates.	**(7)**	**2**	**4**
13. (a)	Design and implement Mod-12 Synchronous up counter using JK flip flops.	**(14)**	**3**	**4**
	(OR)			
(b)	Design a four bit shift registers for SIPO and PISO mode of data transfer.	**(14)**	**3**	**4**
14. (a)	Design an Asynchronous sequential circuit that has two inputs X2 and X1 and one output Z. When X1=0, the output Z is 0. The first change in X2, that occurs while X1 is 1 will cause output Z to be 1. The output Z will remain 1 until X1 returns to zero is 0.	**(14)**	**4**	**4**
	(OR)			
(b)	**(i)** Design a hazard free circuit for the following minterms. $F = \sum m(0,2,6,7,8,10,12)$	**(6)**	**4**	**4**
	(ii) Draw the logic diagram and state table for the following state equations.	**(8)**	**4**	**4**

$$X_1^+ = X_0 I_1 + I_0 X_1$$
$$X_0^+ = X_0 I_1 + \overline{X_1}\,\overline{I_1} I_0 + \overline{X_1} X_0 I_1$$
$$Z = X_0 I_1$$

15. (a)	Implement the following Boolean function with PLA	**(14)**	**5**	**3**

$$w(A,B,C,D) = \sum(2,12,13)$$
$$x(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$$
$$y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$$
$$z(A,B,C,D) = \sum(1,2,8,12,13)$$

	(OR)			
(b)	Implement the NAND and EX-OR gate logic using CMOS Logic.	**(14)**	**5**	**3**

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Design a 32X1 multiplexer logic with 8X1 multiplexers and a decoder.	**(10)**	**2**	**5**

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