Q. Code:547794

Reg. No. | | | | | | | | | | | | |

B.E/B.TECH DEGREE EXAMINATIONS, MAY 2024

Third Semester

EC22302 – DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

(Regulation 2022)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Examine different methods used for simplification of Boolean expressions.	**2**
CO 2	Design combinational logic circuits using logic gates.	**3**
CO 3	Design sequential logic circuits using flipflops.	**3**
CO 4	Investigate and design synchronous and asynchronous sequential circuits.	**4**
CO 5	Apply the digital circuits for solving real world problems and implement the logic function using different types of PLD.	**4**

PART- A (20x2=40Marks)

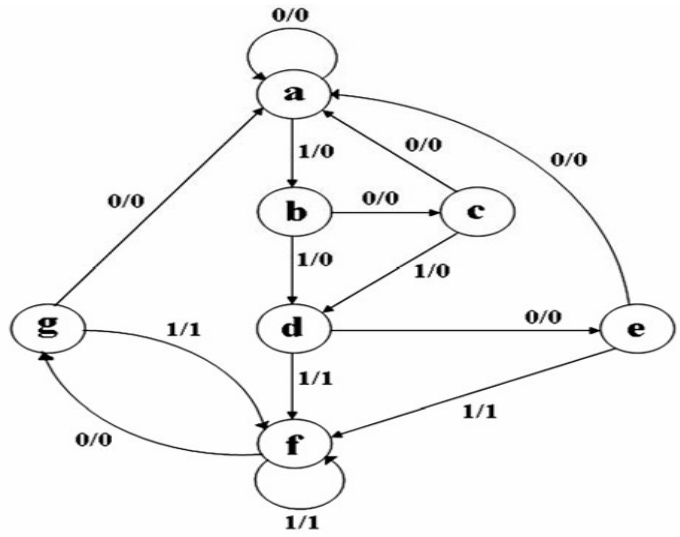
(Answer all Questions)

		CO	RBT LEVEL
1.	Simplify F (A, B) = $A^1B + AB + AB^1$.	**1**	**2**
2.	Express F = Y + XZ in canonical SOP.	**1**	**2**
3.	Implement using NOR gates only, F = $AB + A^1B^1$.	**1**	**2**
4.	What is Principle of Duality?	**1**	**2**
5.	Draw the logic diagram of Half Adder and write its sum and carry expression.	**2**	**2**
6.	What is barrel shifter?	**2**	**2**
7.	Compare demultiplexer and decoder.	**2**	**3**
8.	What is priority encoder?	**2**	**2**
9.	Write the characteristic equation of JK and D flip flop.	**3**	**2**
10.	Convert T flip flop to D flip flop.	**3**	**2**
11.	Differentiate Synchronous and Asynchronous counter.	**3**	**3**
12.	How many flip flop’s are required to build a binary counter that counts from 0 to 511?	**3**	**2**
13.	Compare Mealy and Moore Machines.	**4**	**3**
14.	Define state diagram.	**4**	**2**
15.	Define Race condition.	**4**	**2**
16.	What are Hazards?	**4**	**2**
17.	What is the binary value for 14? Express this in to gray code.	**5**	**3**
18.	Draw the logic circuit of a 1-bit comparator.	**5**	**2**

19.	List the advantages of PLD's.	**5**	**2**	
20.	What are the advantages of pipelined adder?	**5**	**2**	

PART- B (5x10=50Marks)

		Marks	CO	RBT LEVEL
21. (a)	Minimize the following function using K-map. F (A, B, C, D, E) = ∑m (0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27)	**(10)**	**1**	**3**
	(OR)			
(b)	Implement AND, OR , NOT and NOR gate using only NAND gate.	**(10)**	**1**	**3**
22. (a)	Design a BCD adder and explain its working with necessary block diagram.	**(10)**	**2**	**3**
	(OR)			
(b)	Explain the operation of a 8 X 1 Multiplexer and Implement the following function using a suitable Multiplexer. F (A, B, C, D) = ∑m (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)	**(10)**	**2**	**3**
23. (a)	**(i)** Convert JK flip flop in to D flip flop. **(ii)** Convert T flip flop in to JK flip flop.	**(5+5)**	**3**	**3**
	(OR)			
(b)	Design a synchronous counter to count the sequence 0, 4, 2, 1, 6, 0, …. using JK flip flop.	**(10)**	**3**	**3**
24. (a)	Design a synchronous sequential logic circuit using D flip flops for the following state diagram. Use state reduction if possible.	**(10)**	**4**	**3**



(OR)

(b)	Design a Mealy machine for a binary input sequence such that if it has a substring 101, the machine output A, if the input has substring 110, it outputs B otherwise it outputs C.	**(10)**	**4**	**3**
25. (a)	Design a 4-bit binary to gray code converter and draw its logic diagram.	**(10)**	**5**	**3**
	(OR)			
(b)	Design a sequence detector which detects the sequence "01110" (with one bit overlapping) using D flip-flop.	**(10)**	**5**	**3**

PART- C (1x 10=10Marks)

(Q.No.26 is compulsory)

		Marks	CO	RBT LEVEL
26.	Implement a full adder with two 4 x1 Multiplexers.	**(10)**	**2**	**4**

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