Q. Code:140786

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2024

Sixth Semester

EC18601 – VLSI DESIGN

(Electronics and Communication Engineering)

(Regulation 2018/2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Sketch the CMOS logic circuit using Stick Diagrams and Layout Diagrams.	**3**
CO 2	Identify the MOS circuits for various combinational logic blocks and analyze performance parameters.	**3**
CO 3	Develop Sequential logic blocks and perform timing analysis.	**3**
CO 4	Detect suitable MOS logic style for designing arithmetic logic blocks.	**3**
CO 5	Compute FPGA and perform testing.	**3**

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Define body bias effect.	**1**	**2**
2.	By what factor the gate capacitance must be scaled if constant electric field scaling is used?	**1**	**3**
3.	Highlight the feature and drawback of Domino Logic family?	**2**	**2**
4.	Design OR/NOR logic using Differential Pass Transistor Logic.	**2**	**3**
5.	In a bistable circuit, how is the stable state changed from one to another?	**3**	**2**
6.	How does clock gating reduce dynamic power?	**3**	**2**
7.	Define Bit Slicing and bring out the benefits of Bit-Slicing.	**4**	**2**
8.	Analyze the pros and cons of Carry Select Adders.	**4**	**4**
9.	What are the approaches in design for testability/ classification of testing?	**5**	**2**
10.	List the various types of programming technologies used in FPGA design.	**5**	**2**

PART- B (5 x 14 = 70 Marks)

		Marks	CO	RBT LEVEL
11. (a)	Define scaling? What are the various scaling principles widely used? Explain different scaling factors for device parameters and the limitations of scaling.	**(14)**	**1**	**2**
	(OR)			
(b)	With neat diagrams, explain the gate, source and drain formation and isolation steps in fabricating an inverter using p-well CMOS technology	**(14)**	**1**	**2**
12. (a)	Discuss about the signal integrity issues in dynamic design along with the methods to overcome the some of the issues.	**(14)**	**2**	**3**
	(OR)			

(b)	Draw the logic circuit for the given Boolean Expression, using the Logic Family mentioned below and write the ***feature*** and ***limitation*** of the respective logic family. Boolean Function $F=\overline{(A+BC)}$ (1) CMOS Logic (2) Pseudo NMOS (3) Differential Cascode Voltage Switch Logic (DCVSL) (4) Dynamic Gate Logic (5) Domino Logic	**(14)**	**2**	**3**
13. (a)	Draw and explain the operation of a transmission gate mux based positive edge triggered register and analyze for the minimum clock period needed for reliable operation.	**(14)**	**3**	**4**
	(OR)			
(b)	With suitable diagrams explain why the propagation delay of a positive edge triggered True Single Phase Clocked Register, is equal to three inverter delays? What is the setup time for this register? When does this register malfunction?	**(14)**	**3**	**4**
14. (a)	Design a 16-bit Carry Bypass Adder and 16-bit Carry Select Adder and analyze the area and speed trade off.	**(14)**	**4**	**3**
	(OR)			
(b)	Draw the Booth Multiplier Structure with the various important blocks. Justify how Booth algorithm speeds up the multiplication process with an illustration of 6 x 6 multiplication.	**(14)**	**4**	**3**
15. (a)	Explain scan-based testing and highlight the overheads involved.	**(14)**	**5**	**4**
	(OR)			
(b)	Bring out the features in Standard Cell Based ASIC and Gate Array Based ASIC along with the routing procedure for these ASICs.	**(14)**	**5**	**4**

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Discuss about the 'Monotonicity Woes' in cascading Dynamic Logic Circuits with suitable illustration. How is it resolved? (8+2)	**(10)**	**2**	**5**

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