Q. Code: 991283

Reg. No. | | | | | | | | | | | | | |

B.E / B.TECH. DEGREE EXAMINATIONS, MAY 2024

Fifth Semester

EC18503 – COMPUTER ORGANIZATION AND DESIGN

(Electronics & Communication Engineering)

(Regulation 2018 / 2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Compute the performance of various computer architecture and to interpret the instruction set of MIPS processor.	**4**
CO 2	Design and construct various arithmetic circuits for an Arithmetic and Logic units of computing systems.	**4**
CO 3	Assessing various pipelining techniques to implement it for better data path construction for Control units of computing systems.	**3**
CO 4	Categorize various paralleling process techniques and its challenges and also to distinguish various multithreading techniques.	**3**
CO 5	Organize the different Memory technologies and I/O systems to be preferred for computer architectural design.	**4**

PART- A(10x2=20Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Define the terms instruction, operation, and operand in the context of computer architecture.	**1**	**3**
2.	Compare and contrast the characteristics of uniprocessor and multiprocessor systems.	**1**	**3**
3.	Point out the importance of sub-word parallelism.	**2**	**3**
4.	Convert the given decimal number into binary and Express it in IEEE 754 Single Precision Format $(15.250)_d$.	**2**	**3**
5.	Mention the various phase in executing an instruction.	**3**	**2**
6.	A pipeline 'P' operating at 500MHz has a speedup factor of 6 and operating at 75% efficiency. Calculate the number of stages in the pipeline.	**3**	**3**
7.	State the Limitations to increase the clock frequency or processor speed.	**4**	**2**
8.	Discuss the major challenges in parallel processing.	**4**	**3**

9.		Briefly describe the role of Translation Look aside Buffers (TLBs) in virtual memory management.	**5**		**4**
10.		What is the purpose of dirty/ modified bit in cache memory?	**5**		**3**

PART- B (5x 14=70Marks)

			Marks	CO	RBT LEVEL
11. (a)	**i**	Assume variable **h** is associated with register **$s1** and the base address of the array **A** is in **$s2**. What is the MIPS assembly code for the C assignment statement **A[16] = h + A[12];** Also represent all the MIPS code in machine readable format.	**(10)**	**1**	**3**
	ii	Explain in detail the Components of a computer.	**(04)**	**1**	**3**
		(OR)			

(b)	**i**	In the following code segment, f,g,h,i and j are variables which correspond to MIPS registers $s0 to $s4, Write the equivalent MIPS code and elaborate on it.
		if (i==j)
		f= g + h;
		else
		f= g - h;
			(07)	**1**	**3**

	ii	List the eight great ideas in computer architecture and explain with example.	**(07)**		
12. (a)		Demonstrate with examples how floating point addition and multiplication is done in a computer system.	**(14)**	**2**	**4**
		(OR)			
(b)	**i)**	Perform Multiplication operation Using Booth's Algorithm for the given Signed Numbers Multiplicand = $(-7)_{10}$ Multiplier =$(2)_{10}$	**(07)**	**2**	**4**
	ii)	Divide the following numbers using Restoration division technique Dividend(Q) =$(9)_{10}$ Divisor (M)= $(3)_{10}$	**(07)**	**2**	**4**
13. (a)		Describe MIPS data path implementation for an R-type instruction with necessary multiplexers and control lines.	**(14)**	**3**	**2**
		(OR)			
(b)		Describe the data path in operation for a branch-on-equal instruction with suitable block diagram.	**(14)**	**3**	**2**
14. (a)		Demonstrate the three Principal approaches to Hardware Multithreading with necessary diagrams.	**(14)**	**4**	**4**
		(OR)			
(b)		Compare the Michael Flynn's classifications of parallel computing system in terms of instruction and data stream with necessary sketches.	**(14)**	**4**	**4**

		Marks	CO	RBT LEVEL
15. (a)	Discuss in detail the ways for improving cache performance.	**(14)**	**5**	**3**
	(OR)			
(b)	Consider a main memory has 3 page frames 0,1,2. Processors requires pages from virtual memory in the following sequence of page numbers:7,3,7,1,5,7,4,5,3,7,5,7. Show and compare the implementation of FIFO, LRU, LFU page replacement techniques.	**(14)**	**5**	**3**

PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Conduct performance analysis of three types of pipeline hazards and the various techniques used to manage the dependencies in detail.	**(10)**	**5**	**5**