Q. Code:532956

Reg. No. | | | | | | | | | | | | | | |

B.E / B.TECH. DEGREE

EXAMINATIONS, MAY 2024

Third Semester

EC18304 – DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

(Regulation 2018/2018A)

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Analyze different methods used for simplification of Boolean expressions.	**3**
CO 2	Design various Combinational circuits using logic gates.	**2**
CO 3	Analyze and design synchronous and asynchronous sequential circuits.	**3**
CO 4	Design RAM, ROM, PAL and PLA devices.	**3**
CO 5	Write simple HDL codes for digital circuits.	**3**

TIME: 3 HOURS **MAX. MARKS: 100**

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Which gates are called the universal gates? What are its advantages?	**1**	**2**
2.	Prove (x+y)(x'z'+z)(y'+xz)'=x'y	**1**	**3**
3.	Draw the logic diagram of a full subtractor.	**2**	**1**
4.	Compare combinational and sequential circuits.	**2**	**4**
5.	Identify a sequential circuit which uses 4 memory elements and the complemented output of the last memory element is fed as the input to the first memory element and draw the same.	**3**	**4**
6.	How many flip-flops are required to design a counter that counts from 0 to 30?	**3**	**2**
7.	Draw the circuit diagram of 2 input CMOS NOR gates.	**4**	**1**
8.	Implement the Ex-OR function using ROM.	**4**	**4**
9.	Compare critical and non critical races.	**5**	**4**
10.	Write the Verilog code for the half subtractor.	**5**	**2**

PART- B (5 x 14 = 70 Marks)

			Marks	CO	RBT LEVEL
11. (a)		Find the minimal SOP representations for F (A, B, C, D, E) = m (1,4,6,10,20,22,24,26) +d (0,11,16,27) using the K- map method. Draw the circuit of the minimal expression using only NOR gates.	**(14)**	**1**	**3**
		(OR)			
(b)		Minimize the given function using Quine Mc Cluskey method F(A,B,C,D)= Σ(0,2,3,6,7,8,10,11,12,15)	**(14)**	**1**	**3**
12. (a)	**(i)**	Derive the equation of 4-bit carry look-ahead adder and draw its diagram.	**(10)**	**2**	**3**
	(ii)	Design a full subtractor using 2 half subtractors.	**(4)**	**2**	**3**
		(OR)			
(b)		Design a BCD adder that will add two 4-bit numbers and explain its working with the necessary circuit diagram.	**(14)**	**2**	**3**
13. (a)	**(i)**	Design a 2-bit universal shift register	**(8)**	**3**	**3**
	(ii)	How to realize JK flip flop using D flipflop?	**(6)**	**3**	**3**
		(OR)			
(b)		Explain the operation of the master slave flip flop and show how the race around condition is eliminated.	**(14)**	**3**	**3**
14. (a)		Implement the following function using PLA. F1(A,B,C)=Σm(4,5,7) F2(A,B,C) =Σm(3,5,7)	**(14)**	**4**	**3**
		(OR)			
(b)		Design a memory decoder to select 2 numbers of 4 KB EPROM ICs and two numbers of 8 KB RAM ICs.	**(14)**	**4**	**3**
15. (a)	**(i)**	With suitable examples, explain the various problems encountered in asynchronous sequential circuit design and design a hazard free circuit for the given function y = Σm (1,2,4,5,7,12,14,15). justify your answer.	**(10)**	**5**	**4**
	(ii)	Write a Verilog code for 4:1 MUX.	**(4)**	**5**	**4**
		(OR)			
(b)		Design an asynchronous sequential circuit using D flip flop with two inputs A and B to give an output Z=1 when AB=11 but only if A becomes 1 before B.Draw the necessary state diagrams.	**(14)**	**5**	**4**

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Design a synchronous counter using D flip flops that counts the given sequence 000,011,110,111,011,000,…..	**(10)**	**3**	**3**

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