Q. Code:837469

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2024

Third Semester

CS22304 – MICROPROCESSOR AND COMPUTER ARCHITECTURE

(Computer Science and Engineering)

(Regulation 2022)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Understand the flow of instructions and data.	**2**
CO 2	Design and implement programs on 8086 microprocessor.	**2**
CO 3	Design Multiprocessor based System.	**3**
CO 4	Design I/O Interfacing circuits.	**3**
CO 5	Understand the advantages of pipelining and apply them effectively.	**3**

PART- A (20 x 2 = 40 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Differentiate unidirectional & Bidirectional bus.	**1**	**2**
2.	How many unique memory locations are there for 20-bit address memory?	**1**	**3**
3.	State the difference between Big endian & Little endian assignments.	**1**	**2**
4.	What is the role of cache memory?	**1**	**2**
5.	Differentiate between SUB & CMP instruction.	**2**	**2**
6.	List the flags available in 8086 processor.	**2**	**2**
7.	Differentiate Macros and Procedures.	**2**	**2**
8.	What is the purpose of DT assembler directive?	**2**	**3**
9.	List the use of HLDA/HOLD.	**3**	**2**
10.	Mention the uses of T_w.	**3**	**3**
11.	List the various bus allocation schemes.	**3**	**2**
12.	Define set up time.	**3**	**2**
13.	What is BSR mode in 8255?	**4**	**2**
14.	What is 2-Key roll over?	**4**	**2**
15.	What is Loosely coupled system?	**4**	**2**
16.	Write the control word for programming all the ports acted as a output port.	**4**	**3**
17.	What is the need for pipelining?	**5**	**2**
18.	What is structural hazard?	**5**	**2**
19.	What is operand forwarding?	**5**	**2**

20.	Draw the 4 stage pipelining.		**5**	**3**

PART- B (5 x 10 = 50 Marks)

		Marks	CO	RBT LEVEL
21. (a)	Explain in detail about the operational concept between memory and processor with various components.	**(10)**	**1**	**3**
	(OR)			
(b)	With suitable examples, Describe about various addressing modes.	**(10)**	**1**	**3**
22. (a)	Explain in detail about 8086 microprocessor architecture with a neat diagram.	**(10)**	**2**	**2**
	(OR)			
(b)	Illustrate various data transfer and arithmetic instruction set of 8086 microprocessor with suitable examples.	**(10)**	**2**	**2**
23. (a)	With a neat sketch explain how memory read and write operation is performed in minimum mode of 8086.	**(10)**	**3**	**3**
	(OR)			
(b)	With a neat sketch explain in detail about various bus allocation schemes.	**(10)**	**3**	**3**
24. (a)	With a neat sketch explain in detail about the parallel communication interface - 8255.	**(10)**	**4**	**3**
	(OR)			
(b)	Explain in detail about the Master-Slave operation of the interrupt controller.	**(10)**	**4**	**3**
25. (a)	Define Data hazard. How will you handle dependencies in data hazards?	**(10)**	**5**	**3**
	(OR)			
(b)	Explain modified data path using inter-stage buffers.	**(10)**	**5**	**3**

PART- C (1 x 10 = 10 Marks)

(Q.No.26 is compulsory)

		Marks	CO	RBT LEVEL
26.	How is cycle stealing done with DMA controller? Explain it in detail with a neat diagram.	**(10)**	4	**5**