Q. Code:316767

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH DEGREE EXAMINATIONS, MAY 2024

Second Semester

CS22202 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to CS & AD)

(Regulation 2022)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Students will be able to learn the different types of number systems and simplification of Boolean functions	**1**
CO 2	Students will be able to understand various logic gates and their usage	**2**
CO 3	Students will be able to study, analyze and design various combinational circuits and its implementation using VHDL	**4**
CO 4	Students will be able to understand the different type of memory and their structures	**2**
CO 5	Students will be able to study, analyze of RTL notation register operations in a clocked sequential circuit	**4**

PART- A (20 x 2 = 40 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Simplify the following Boolean Function F=X'Y'+XY+X'Y.	**1**	**1**
2.	What are the limitations of K-map?	**1**	**1**
3.	State and Prove Involution law.	**1**	**1**
4.	Convert the following Decimal$(0.6875)_{10}$ to Binary.	**1**	**1**
5.	Define Combinational circuits.	**2**	**2**
6.	Write the Truth Table for full adder.	**2**	**2**

7.	Write short notes on propagation delay.	**2**	**2**
8.	Design a 1-bit magnitude comparator.	**2**	**2**
9.	Differentiate between latches and flip flops.	**3**	**3**
10.	What is meant by edge triggered flip flops?	**3**	**3**
11.	Summarize the characteristic table and equation of JK flip flop.	**3**	**3**
12.	What is shift register and Classify its types?	**3**	**3**
13.	A seven bit Hamming code is received as 1111110.What is the correct code?	**4**	**2**
14.	List the major difference between PLA and PAL.	**4**	**2**
15.	What is volatile memory? Give an example.	**4**	**2**
16.	How many check bits are required for single bit error detection and correction?	**4**	**2**
17.	Discuss briefly about register transfer level.	**5**	**3**
18.	Identify the modeling techniques available in HDL.	**5**	**3**
19.	Differentiate LOGICAL AND and BITWISE AND operators.	**5**	**3**
20.	Define a Sequential Binary multiplier?	**5**	**3**

PART- B (5 x 10 = 50 Marks)

			Marks	CO	RBT LEVEL
21. (a)	**(i)**	Minimize the following expression using Karnaugh Map	**(5)**	**1**	**1**

Y=A'BC'D'+A'BC'D+ABC'D'+A'B'CD'

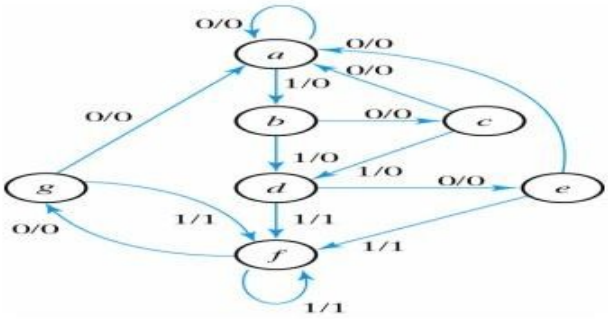
	(ii)	State and Prove Demorgan's theorem	**(5)**	**1**	**1**

(OR)

(b)		Simplify the following switching functions using Quine McCluskey's tabulation method and realize expression using gates F(A,B,C,D) = Σ(0,5,7,8,9,10, 11, 14,15)	**(10)**	**1**	**1**
22. (a)		Design and implement a Binary to gray code converter.	**(10)**	**2**	**2**

(OR)

(b)		Construct a 2 X 4 Encoder and Decoder in detail	**(10)**	**2**	**2**
23. (a)		Reduce the number of states in the following State Table. Construct the reduced state table and draw the state diagram.	**(10)**	**3**	**3**



(OR)

(b)		Design a three bit synchronous counter using JK flip flop. Explain about the execution table and State Table	**(10)**	**3**	**3**
24. (a)		Implement the following using PAL F1(A,B,C)= ∑(1,2,4,6); F2(A,B,C) =∑(0,1,6,7) ; F3(A,B,C)= ∑(1,2,3,5,7)	**(10)**	**4**	**2**

(OR)

(b)		Explain about error detection and correction using hamming codes.	**(10)**	**4**	**2**
25. (a)		Illustrate the HDL operators with their symbol and type of operation performed in RTL.	**(10)**	**5**	**3**

(OR)

		Marks	CO	RBT LEVEL
(b)	Illustrate the Algorithmic State Machine chart in detail.	**(10)**	**5**	**3**

PART- C (1 x 10 = 10 Marks)

(Q.No.26 is compulsory)

		Marks	CO	RBT LEVEL
26.	Construct the following Boolean function using 8:1 multiplexer $F(A,B,C)=\sum(1,3,5,6)$.	**(10)**	**2**	**2**

****